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FINAL REPORT
IUS/PAYLOAD COMMUNICATION SYSTEM SIMULATOR CONFIGURATION
DEFINITION STUDY

Contract No. NAS 9-15409

Prepared for
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ACRONYMS AND SYMBOLS

ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
AM	Amplitude Modulation
BER	Bit Error Rate
BPF	Bandpass Filter
BPL	Bandpass Limiter
bps	Bits per Second
CDU	Command Detector Unit
CIC	Computer Input Converter
CIU	Communication Interface Unit
CMDS	Commands
COC	Computer Output Converter
CIU	Communication Interface Unit
CMDS	Commands
DAC	Digital-to-Analog Converter
DAL	Data-Aided Loop
DOD	Department of Defense
DS	Deep Space
DSN	Deep Space Network
DTTL	Data Transition Tracking Loop
E_b	Energy per Bit
E_s	Energy per Symbol
ESTL	Electronic Systems Test Laboratory
FET	Field Effect Transistor
FM	Frequency Modulator
GCA	Gain Controlled Amplifier
GFE	Government Furnished Equipment
HPF	Highpass Filter
I	In-Phase
IC	Integrated Circuit
IF	Intermediate Frequency
IFA	Intermediate Frequency Amplifier
IIU	Input Interface Unit

I/O	Input/Output
IRIG	Inter-Range Instrumentation Group
IUS	Interim Upper Stage
JSC	Johnson Space Center
LPF	Lowpass Filter
LSI	Large Scale Integration
MFR	Multi-Function Receiver
MFSK	Multiple Frequency Shift Keying
MUX	Multiplexer
NASA	National Aeronautics and Space Administration
NE	Near Earth
N_0	Noise Spectral Density
NRZ	Non-Return to Zero
OIU	Output Interface Unit
PAM	Pulse Amplitude Modulation
p_e^b	Bit Error Probability
p_e^s	Symbol Error Probability
PI	Payload Integrator
PLL	Phase-Locked Loop
PS	Payload Simulator
P/S	Parallel to Serial
PSK	Phase Shift Keying
PSP	Payload Signal Processor
Q	Quadrature-Phase
RF	Radio Frequency
RMS	Root Mean Square
ROM	Read Only Memory
S/C	Subcarrier
SCE	Spacecraft Command Encoder
SGLS	Space Ground Link Subsystem
SNR	Signal-to-Noise Ratio
S/P	Serial to Parallel
sps	Symbols per Second
SRD	Step Recovery Diode
STDN	Space Tracking and Data Network

TBD	To Be Determined
TBS	To Be Supplied
TDRSS	Tracking & Data Relay Satellite System
TLM	Telemetry
TTL	Transistor-Transistor Logic
USAF	United States Air Force
VCO	Voltage Controlled Oscillator
VCXO	Voltage Controlled Crystal Oscillator
VSWR	Voltage Standing Wave Ratio
VVA	Voltage Variable Attenuator or Amplifier

1.0 EXECUTIVE SUMMARY

1.1 Purpose of the Study and Results Presented in This Report

The study involved an investigation of the requirements and specifications for a general purpose payload communications system simulator to be used in the JSC Electronic Systems Test Laboratory (ESTL). This simulator will be used to emulate those communications system portions of NASA and DOD payloads/spacecraft that will in the future be carried into Earth orbit by the Shuttle.

For the purpose of on-orbit checkout, the Shuttle is required to communicate with the payloads while they are physically located within the Shuttle bay (attached) and within a range of 20 miles from the Shuttle after they have been deployed (detached). For this purpose, the following Shuttle major avionic subsystems will be used.

1. Payload Interrogator (PI)
2. Payload Signal Processor (PSP)
3. Communication Interface Unit (CIU)
4. Ku-Band Signal Processor.

As a part of the engineering development of these avionic subsystems plus the establishment of overall system performance characteristics and procedures, it is necessary to fully exercise the avionic equipment with the corresponding payload counterparts. The applicable payloads are

- 1 Intermediate Upper Stage (IUS)
2. NASA near-earth and deep-space vehicles
- 3 DOD spacecraft
- 4 Spacelab

Since many of the payloads are also under development (and many have yet to be defined), actual payload communication hardware will not be available within the time frame during which the avionic hardware tests will be conducted in the ESTL. Thus, a flexible payload communication system simulator [hereafter referred to as the payload simulator (PS)] is required

The study and its results reported herein concentrated on:

1. Determining PS requirements,
2. Examining methods for PS implementation,
3. Specifying a PS design,
4. Estimating the cost of the PS, and
5. Outlining PS usage and testing criterion.

1.2 Study Objectives and Results

The primary objectives/results of the effort were:

1. Prepare a comprehensive report (this report) of the PS requirements, design, implementation, tradeoffs, and usage.
2. Generate a detailed design and performance specification (Appendix A of this report) for use in procuring the PS.
3. Provide cost estimates (separate cost volume of this report), by subsystem, of the PS hardware.

Three secondary goals of the study program involved:

1. Outlining the types and nature of the system tests that will be performed using the PS
2. Establishing the ESTL/PS interfaces
3. Providing ESTL integration and checkout procedures.

The results pertaining to all of these items may be found in this report

1.3 Study Approach

The early phases of the study concentrated on establishing the salient PS requirements based upon the following inputs:

1. JSC Task 501 documents and objectives
2. IUS communication system configuration
 - a. Boeing documents
 - b. Discussions with SAMSO
3. Typical NASA payloads
 - a. NASA standard transponders and command detector specifications
 - b. JPL mission configurations
 - c. GSFC mission configurations
 - d. Spacelab documents

4. Typical DOD payloads
 - a. SGLS documents
 - b. Discussions with SAMSO

With the PS requirements ascertained, the effort was next concentrated on determining the current and potential PS interfaces. This was accomplished by investigating:

1. Shuttle avionic equipment
 - a. JSC documents
 - b. Rockwell documents
2. ESTL equipment
 - a. ESTL configuration documents
 - b. Discussions with JSC personnel

The bulk of the study was concerned with design and implementation considerations and tradeoffs such as:

1. Diverse subsystem configurations versus maximum functional circuit and equipment commonality
2. Maximum application of existing designs.
3. Extensive use of commercial equipment and assemblies
4. Modification of existing ESTL equipment.
5. Flexibility, operating factors, and change/growth.
6. Cost minimization.

Upon completion of the design phase, the proposed design was documented (this report) and a specification prepared (Appendix A of this report). For maximum utility, the specification (1) is organized by major PS subsystems, (2) specifies all performance, interface and operational parameters, and (3) details the design approach to the functional level

Finally, the PS subsystems were costed using an algebraic cost model based upon major component costs and engineering/fabrication labor.

1.4 Payload Simulator Subsystems and Physical Configuration

Figure 1-1 shows the PS/ESTL generic block diagram. The PS itself is comprised of the four equipment assemblies to the left of the dashed line.

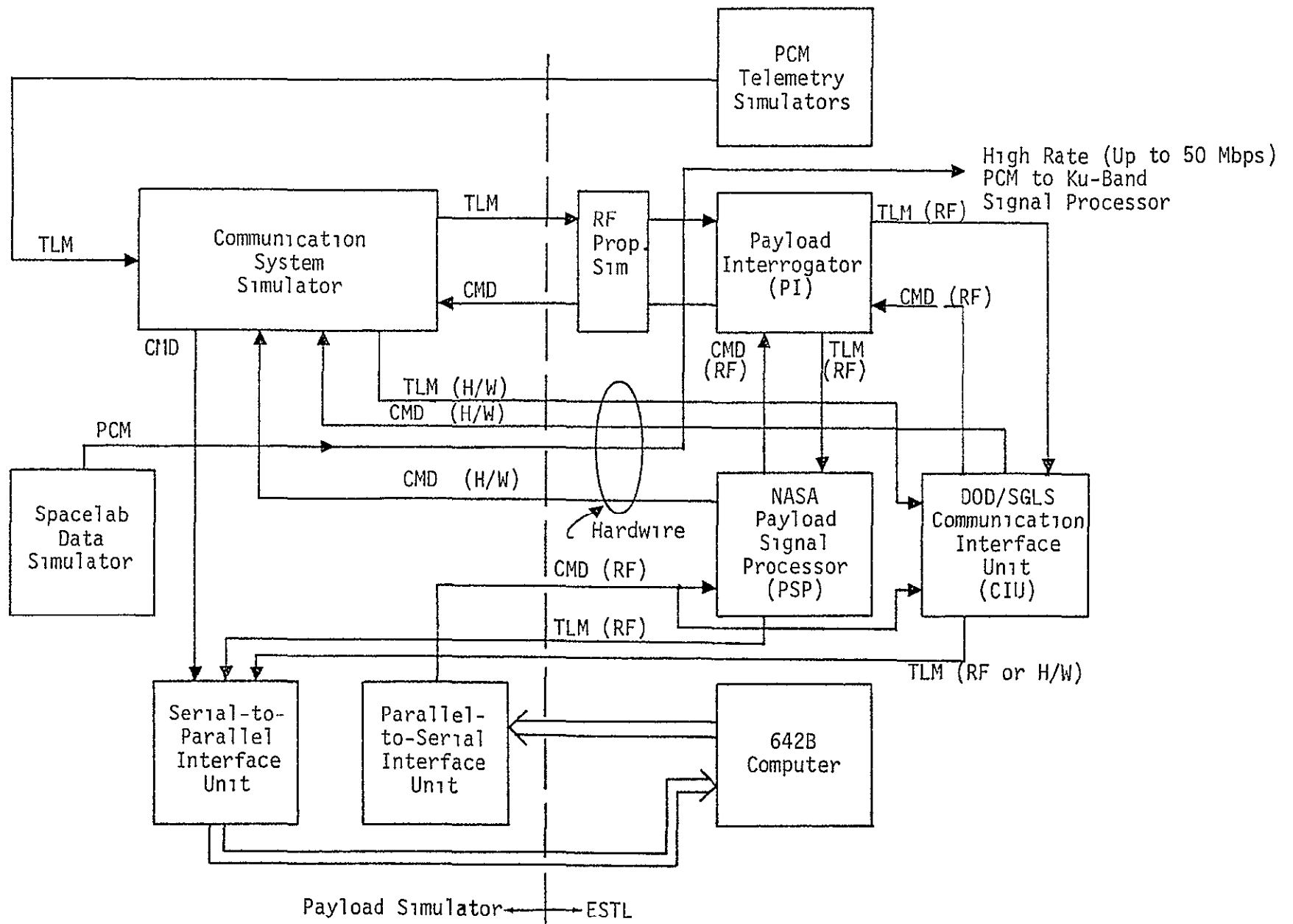


Figure 1-1 Payload Simulator/ESTL Generic Block Diagram

The Communication System Simulator is by far the most extensive piece of equipment, being comprised of the

1. Transponder
 - a. Receiver
 - b. Transmitter
 - c. Frequency synthesizer
2. Command Detector Unit
 - a. NASA detector
 - b. SGLS detector
3. Telemetry Modulator
 - a. Subcarrier PSK modulator
 - b. Subcarrier frequency modulator
4. Command/telemetry multiplexer

All of this hardware will be configured in a rack cabinet as shown in Figure 1-2 and will be located in ESTL shielded enclosure #3.

The interface units used to transfer digital data between the 642B computer, PS and avionic equipment, will be located near the 642B computer in the ESTL.

A piece of existing ESTL hardware will be modified to provide the Spacelab data simulator function.

An overview description of the PS and ESTL equipment is given in Section 2.0, and design details of the PS subsystems may be found in Section 4.0 of this report. Conceptual subsystem panel configurations and operating features are found in Section 7.0.

1.5 Payload Simulator Cost Summary

(See separate Cost Volume.)

1.6 Open-Items, Additional Considerations, and Recommendations

During the course of the study, nearly all requirements were firmly established. However, certain issues were not fully resolved due primarily to the fact that some future payload capabilities have not been clearly established by the cognizant agencies. From among these items, the most important are.

1. Ranging requirements

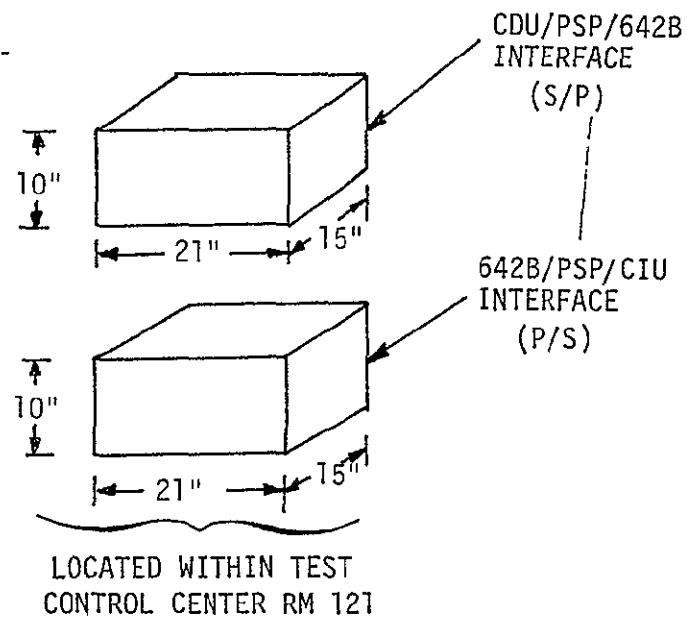
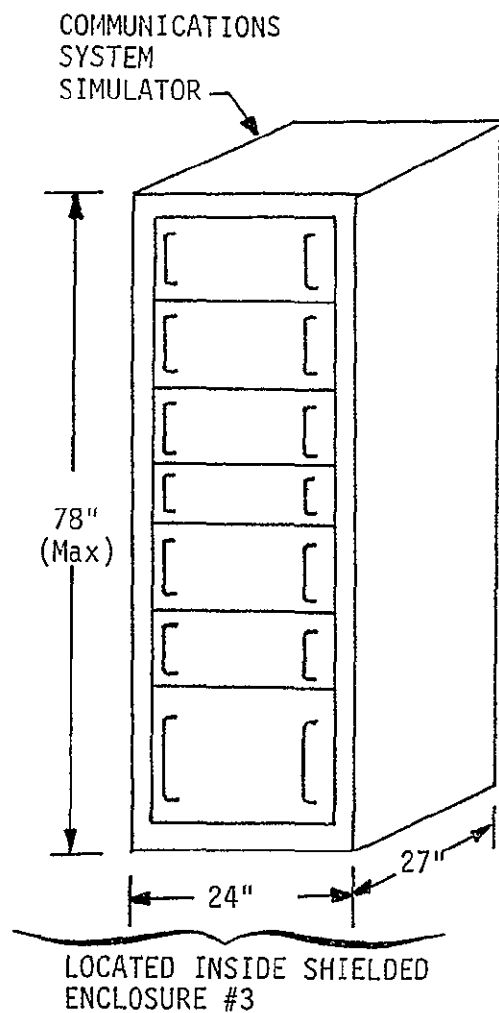


Figure 1-2. Payload Simulator Equipment Assemblies

2. Nature of test configurations involving DOD COMSEC equipment.
3. Complete command/telemetry multiplexing definition.
4. Receiver swept frequency acquisition.
5. Extent of SGLS FM capability required

These issues should be further studied and resolved as they impact the PS design and have significant cost implications.

In Sections 3.0 and 5.6 of the report, the nature of the tests to be performed on and with the PS are delineated. Many of these tests can be made using commercial and existing ESTL equipment. Others, however, require special hardware configurations and techniques. Performance of these latter tests using sampled-data instrumentation has been studied and summarized in Appendix C of this report. As the sampled-data approach appears to be highly flexible and cost effective, it should be given further consideration and definition.

Finally, ESTL integration and checkout of the PS is outlined in Section 5.0. Although certain details are provided, a step-by-step integration and checkout procedure must realistically be generated during the PS implementation activity if it is to be useful. It should include a detailing of test methods and procedural commentary.

2.0 SIMULATOR OVERVIEW FUNCTIONAL DESCRIPTION

2.1 General ESTL and Simulator Configuration

A main objective of the NASA Task 501 Program is the verification testing of the various RF space-space and space-ground links of the Shuttle and Shuttle-launched payloads. A considerable portion of this verification testing will be performed by the Johnson Space Center's Electronic Systems Test Laboratory (ESTL).

The functional diagram of the ESTL is shown in Figure 2-1. As can be seen from this diagram, the ESTL has the capability to simulate the direct Shuttle/earth S-band links and the indirect Orbiter/ground S-band and Ku-band links. Means are additionally provided to simulate the data generated within the Orbiter itself, along with the capability for routing it via the various space-ground links for the purpose of total systems evaluation.

The Orbiter communications subsystem provides a capability for establishing communication links with both attached payloads within the Shuttle bay and detached payloads in the near vicinity of the Orbiter. Communication with attached payloads is via hardwire channels which typically include at least one forward link from the Orbiter for commands and one return link for telemetry. The detached payload RF communication is a two-way link carrying commands, telemetry, and sometimes ranging. Both the hardwire and RF links with the payload constitute a portion of the overall space-space capability of the Orbiter communication system.

Typical payloads with which the Orbiter communications system must be capable of interfacing are:

- Intermediate Upper Stage (IUS),
- NASA near-earth spacecraft,
- NASA deep-space spacecraft,
- USAF satellites (especially those to be placed in orbit by the IUS),
- Spacelab

The RF signal and modulation structures of all payload communications systems are standardized to be compatible with the Orbiter Payload Interrogator (PI) and Payload Signal Processor (PSP). Additionally,

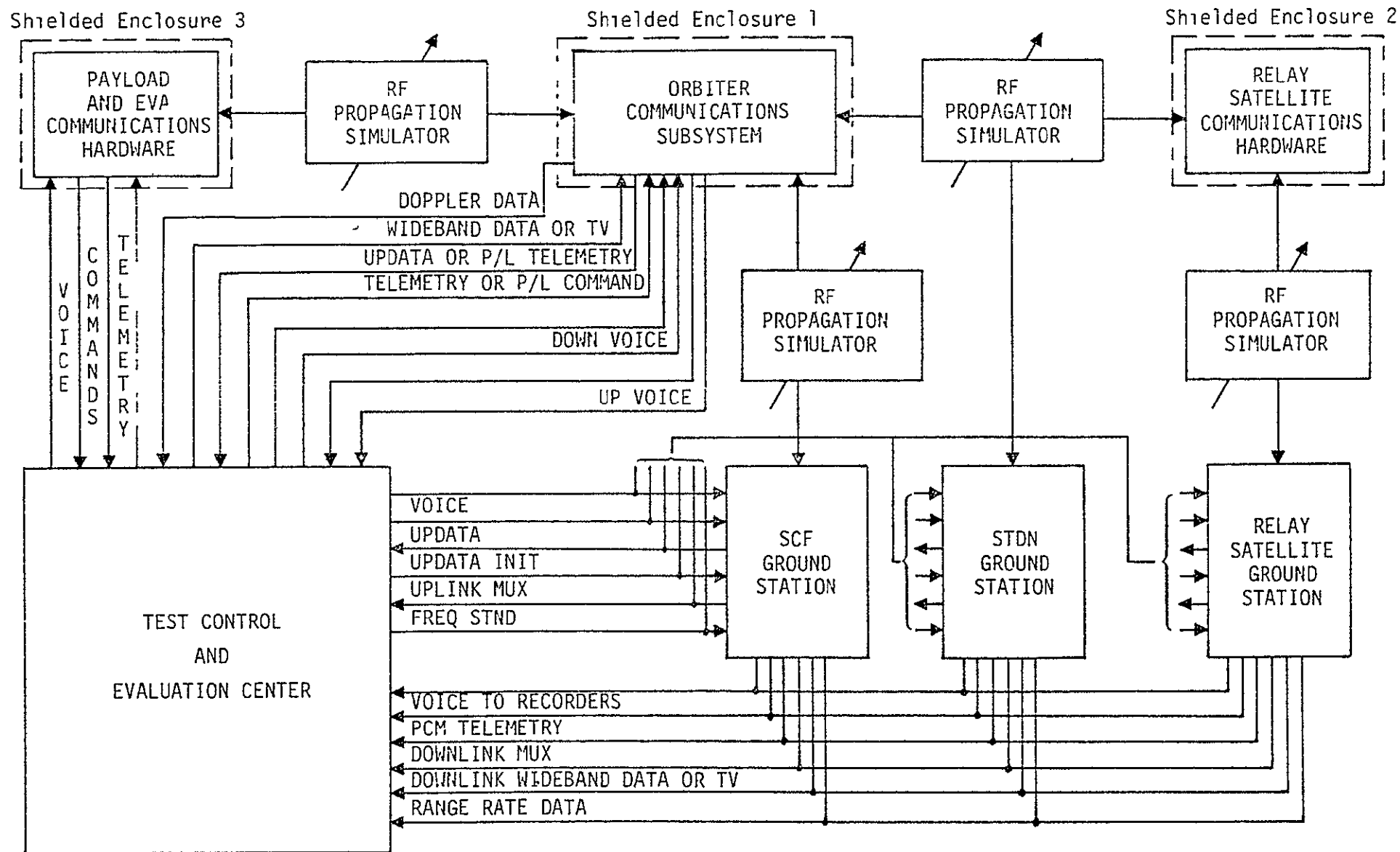


Figure 2-1 ESTL Functional Block Diagram

fixed data rates and formats are required of RF and hardwire command and telemetry information.

The capability of the ESTL to evaluate payload communication functions is enhanced by the use of special-purpose test equipments which emulate the electrical characteristics of the actual payloads. One such piece of equipment is the Payload Simulator which provides the requisite RF and hardline capability to fully exercise the PI and PSP.

The design, specification, and operation of the Payload Simulator is the subject of this report.

2.1.1 Payload Simulator Functions and Interfaces

The Payload Simulator (PS) is a piece of test equipment that will be located within one of the shielded enclosures of the ESTL. The prime function of the PS is to simulate those payload communication system configurations that will at some future time operationally interface with the PI [1], the PSP [2], the Ku-Band Processor and, for DOD payloads, the Communication Interface Unit (CIU). The manner by which the PS provides ESTL test capability augmentation is illustrated by the block diagram of Figure 2-2. The blocks shown within and to the left of the dotted line are those comprising the overall PS equipment.

The signal interfaces which exist between the ESTL and the PS are of three basic types:

- (1) Radio frequency (RF)
- (2) Hardwire signal lines
- (3) Test support lines

The hardwire and RF interfaces provide for simulating the attached and detached payloads, respectively. Test support interfaces provide signal flow loops between the sources of test data and the points of data verification.

Much of the NASA configuration testing makes use of the ESTL Univac 642B computer [3]. Since the interfaces with the PSP and the PI are serial, appropriate interface units are therefore provided as a part of the PS equipment. For testing of the forward (Orbiter-payload) link, the computer generates commands which are sent to the payload via either a cable (hardwire) or the simulated RF link. Command verification

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is performed by the 642B computer. Return link (payload-Orbiter) telemetry data is originated by either the PCM telemetry simulator or a tape recorder, and transmitted via cable or RF. PCM simulator data is usually verified directly by a bit error comparator, while tape recorder-generated data must be tested by the 642B computer for known pattern errors.

The use of the 642B computer in conjunction with DOD CIU/PI testing depends on the nature of the tests to be carried out. Primarily, it is used to aid in the statistical evaluation of the link performance. The computer may also be employed to provide simulated navigation update signals for transmission to the PS. Most importantly, the 642B provides the processing and control necessary to multiplex received commands and return telemetry data, with the CIU ultimately being used to perform command verification.

Table 2-1 gives a summary of the link test configurations which the PS will provide for ESTL testing of the Orbiter communications subsystems.

Table 2-2 lists the PS communication and support functions. Descriptions of the major subsystems are found beginning at Section 2.2.

2.1 2 Shuttle Avionic and ESTL Equipment and Functions

2.1 2.1 Payload Interrogator

The PI is basically an RF transmitter and receiver. Either an actual flight unit or an equivalent prototype PI will be employed within the ESTL.

The PI provides for the Orbiter end of the RF link to/from the payload. This RF link must accommodate, on a nonsimultaneous basis, signals compatible with NASA and DOD/SGLS (hereafter simply referred to as SGLS) modes. Both simplex and duplex communication with the payloads are required.

The RF capability of the PI works over 851 duplex channels consisting of 20 SGLS mode channels with a turnaround ratio of 256/205 and 831 NASA channels with a turnaround ratio of 240/221. The transmit frequency range of the PI is in two bands. L-band (1760-1840 MHz) and S-band (2025-2120 MHz). The corresponding range of the receive frequencies is from 2200 to 2300 MHz. With respect to other avionic equipment,

Table 2-1. Summary of IUS/Payload Equipment and ESTL Communication Link Test Configurations

User	Link Type	Data	Modulation Format	Signal Test Function	Signal Flow Direction Tested (Simulated)
NASA	Hardwire	CMDS	NRZ	Payload CDU Bit Detector	Orbiter to Payload
	Hardwire	CMDS	PSK	Payload CDU Performance	Orbiter to Payload
	Hardwire	TLM	NRZ	Ku-Band Processor	Payload to Orbiter
	RF	CMDS	PSK/PM	PI and PSP	Orbiter to Payload
	RF	TLM	PSK/PM	PI and PSP	Payload to Orbiter
DOD	Hardwire	CMDS	Ternary Symbols plus Clock	CIU	Orbiter to Payload
	Hardwire	CMDS	FSK/AM	CIU and Payload CDU	Orbiter to Payload
	Hardwire	NAV UPDATE	PSK	PSP/CIU	Orbiter to Payload
	Hardwire	TLM	NRZ	CIU	Payload to Orbiter
	Hardwire	TLM	PSK or FM	CIU	Payload to Orbiter
	RF	CMDS	FSK/AM/PM	PI and CIU	Orbiter to Payload
	RF	TLM	PSK/PM or FM/PM	PI and CIU	Payload to Orbiter

Table 2-2. Simulator Function Categories

Simulated Communication Functions	Support Functions
RF Receiver Frequency Source/Exciter Phase Modulator Power Amplifier	Serial to Parallel Data Converter(s) Parallel to Serial Data Converter
Subcarrier Generators Subcarrier Modulators	Univac 642B Input and Output Equipment
Command Subcarrier Demodulator Command Bit Detector	Special Test Equipment
Command and Telemetry Multiplexer	Payload Hardware Interface Equipment
High Data Rate (50 Mbps) Data Generator	

the PI interfaces with the NASA PSP and the DOD CIU. The PSP biphase modulates the commands onto a 16 kHz subcarrier and delivers them to the PI transmitter. The PI receiver provides received and carrier demodulated telemetry on a 1.024 MHz subcarrier to the PSP unit. In the DOD mode, the PI receives FSK commands from the CIU and returns telemetry to the CIU on either a 1.024 MHz or a 1.7 MHz subcarrier.

2.1.2.2 NASA Payload Signal Processor

One function of the PSP is to receive and configure command messages from external sources, modulate them onto a 16 kHz subcarrier, and supply the composite signal to the PI. The PSP also receives the telemetry data from the PI on a 1.024 MHz subcarrier, demodulates it, and detects and supplies the telemetry bit stream to the Payload Data Interleaver. For the testing phase involving the PS, however, the telemetry is transferred to the 642B computer for statistical evaluation of the link error rates.

The PSP is also used to generate baseband signals to the attached payload. A hardwire interface carries commands to the payload in the form of biphase modulation on a 16 kHz subcarrier.

2.1.2.3 DOD Communication Interface Unit

The CIU performs functions analogous to the NASA PSP. Thus, the CIU provides for command and telemetry signal selection, routing, and formatting, plus subcarrier modulation and demodulation. The CIU additionally performs such DOD specialized functions as command signal authentication/verification and flight crew-initiated command generation.

In the attached mode, the CIU generates and outputs via hardware the following signals to the payload:

- (1) Baseband command modulation (FSK/AM)
- (2) "S," "0," and "1" command symbols plus clock (4 lines)
- (3) NRZ-L commands on a 16 kHz subcarrier. (The command rates for this signal will be in the NASA formats and at one of the nine NASA rates.)

Also in the attached mode, the CIU receives the following telemetry signals from the payload:

- (1) 1.024 MHz PSK modulated subcarrier
 - (2) 1.7 MHz PSK modulated subcarrier
 - (3) 1.7 MHz FM/FM or PAM/FM modulated subcarrier
 - (4) Up to 64 kbps baseband TLM NRZ data
 - (5) Up to 256 kbps baseband TLM NRZ data
- } Separate inputs

When operating with the detached payload, the CIU interfaces with the PI. The commands to the payload are sent via the PI unit in the SGLS modulation format, FSK/AM ("S" = 65 kHz, "0" = 76 kHz, "1" = 95 kHz)

Telemetry data from the payload is sent to the CIU via the PI on either a 1.024 MHz or 1.7 MHz PSK modulated subcarrier and/or a 1.7 MHz FM subcarrier

Command authentication is performed within the CIU by comparing the commands arriving within the telemetry stream from the payload with the commands originally sent out to the payload. The function of introducing the commands into the telemetry at the payload is done by the PCM telemetry multiplexer (MUX) unit.

2.1.2.4 RF Propagation Path Simulators

RF propagation path simulators are available within the ESTL facility. These units are used to provide very low power RF signal

paths between transmitters and receivers. Of particular importance is the Payload-Orbiter RF link simulator, which consists of RG-214 coaxial cable links to and from a variable attenuator. The variable attenuator provides up to 120 dB of selectable attenuation.

2.1.2.5 Univac 642B Computer

The 642B computer is a general-purpose machine within the ESTL used for data generation, control, formatting, and test diagnostic functions. Its data interfaces require 30-bit parallel word transfers; thus, serial-to-parallel and parallel-to-serial data converters are required when the computer is used with avionic or simulated hardware of the types discussed in the above subsections. Data transfer is executed using interrupt control programs.

2.2 Transponder

A basic block diagram of the PS transponder is shown in Figure 2-3. Each of the major blocks is described in the following subsections, along with the general performance requirements. Note that the PS transponder does not have a diplexer and that the combination of the phase modulator and power amplifier comprise what is known as the transmitter.

2.2.1 Receiver (Figure 2-4)

The forward link RF input is preselected (filtered) for each input frequency band (S-band for NASA and L-band for IUS, DOD/SGLS). The input is then mixed down to the first IF. Further mixing translates the first IF signal to the second IF.

The output from the second IF amplifier is distributed to four phase detector/demodulator functions.

The carrier tracking loop functions to acquire and track the residual carrier component of the input signal. Frequency and phase coherence is supplied from the VCO to the synthesizer/exciter (2.2.2) where the coherent reference frequencies are derived for the demodulation functions. A second-order tracking loop is employed, with sweep acquisition capability available as an option (normally used on SGLS-compatible payloads only).

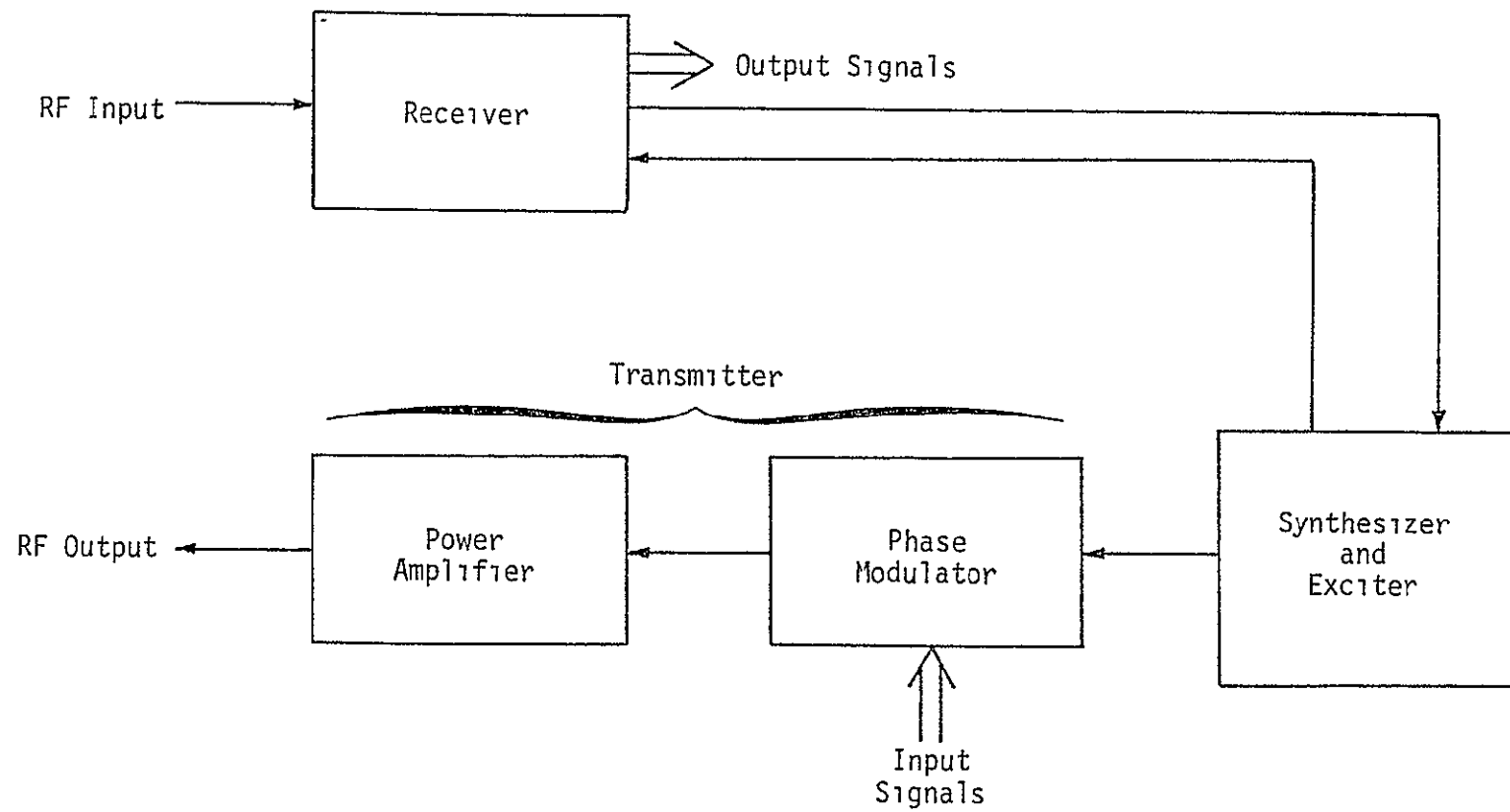


Figure 2-3. PS Transponder

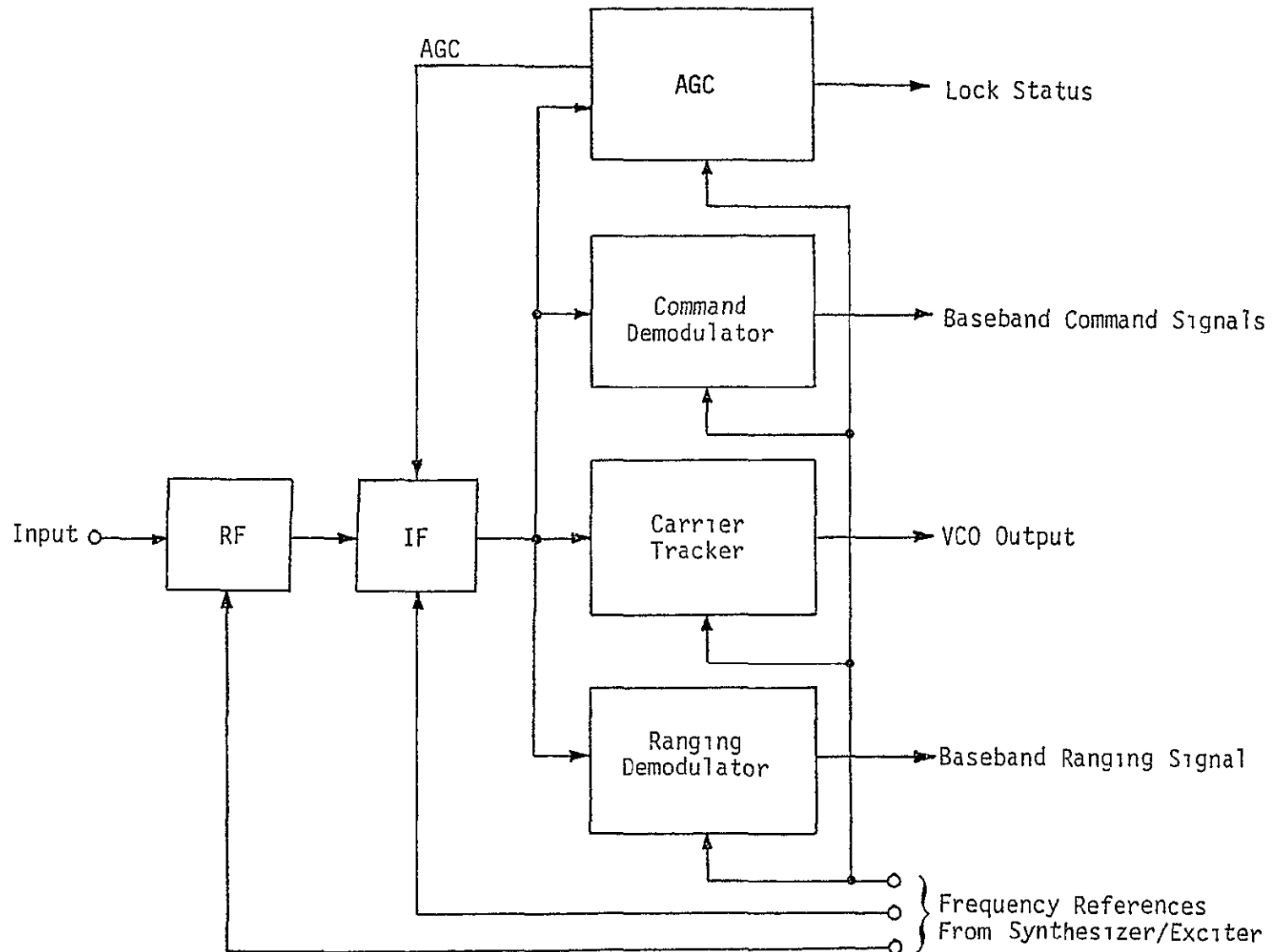


Figure 2-4. PS Receiver

A command demodulator coherently recovers the command phase modulation from the carrier. Spectral conditioning is provided in the output

The ranging demodulator coherently recovers the ranging phase modulation from the carrier. Two post-demodulation amplitude processors are provided. (1) a lowpass hard-limiter and (2) an envelope referenced AGC

AGC is derived through in-phase demodulation of the residual carrier. The AGC voltage is filtered and applied to the first IF amplifier to control the gain of the receiver. AGC voltage is also filtered and compared with a threshold to determine whether the carrier tracking loop is in or out of lock.

Major receiver design and performance parameters are summarized in Table 2-3.

Table 2-3. Receiver Parameters

Item	Parameter and Range
L-Band Frequencies	1760 - 1840 MHz
S-Band Frequencies	2025 - 2120 MHz
Tracking Loop Bandwidth Range	10-2000 Hz
Tracking Loop Order	Second
AGC Dynamic Range	100 dB
Command Channel Frequency Response	1 kHz to 130 kHz
Ranging Channel Frequency Response	1 kHz to 1.2 MHz
Noise Figure	15 dB (maximum)
Minimum Signal Sensitivity	-148 dBm

2.2.2 Synthesizer/Exciter (Figure 2-5)

The synthesizer/exciter provides all reference frequencies to the transponder. A reference oscillator supplies standard frequencies to the receiver synthesizer. The coherence frequency is provided by the receiver VCO. Receiver synthesizer frequencies are distributed to the receiver mixers and phase detectors.

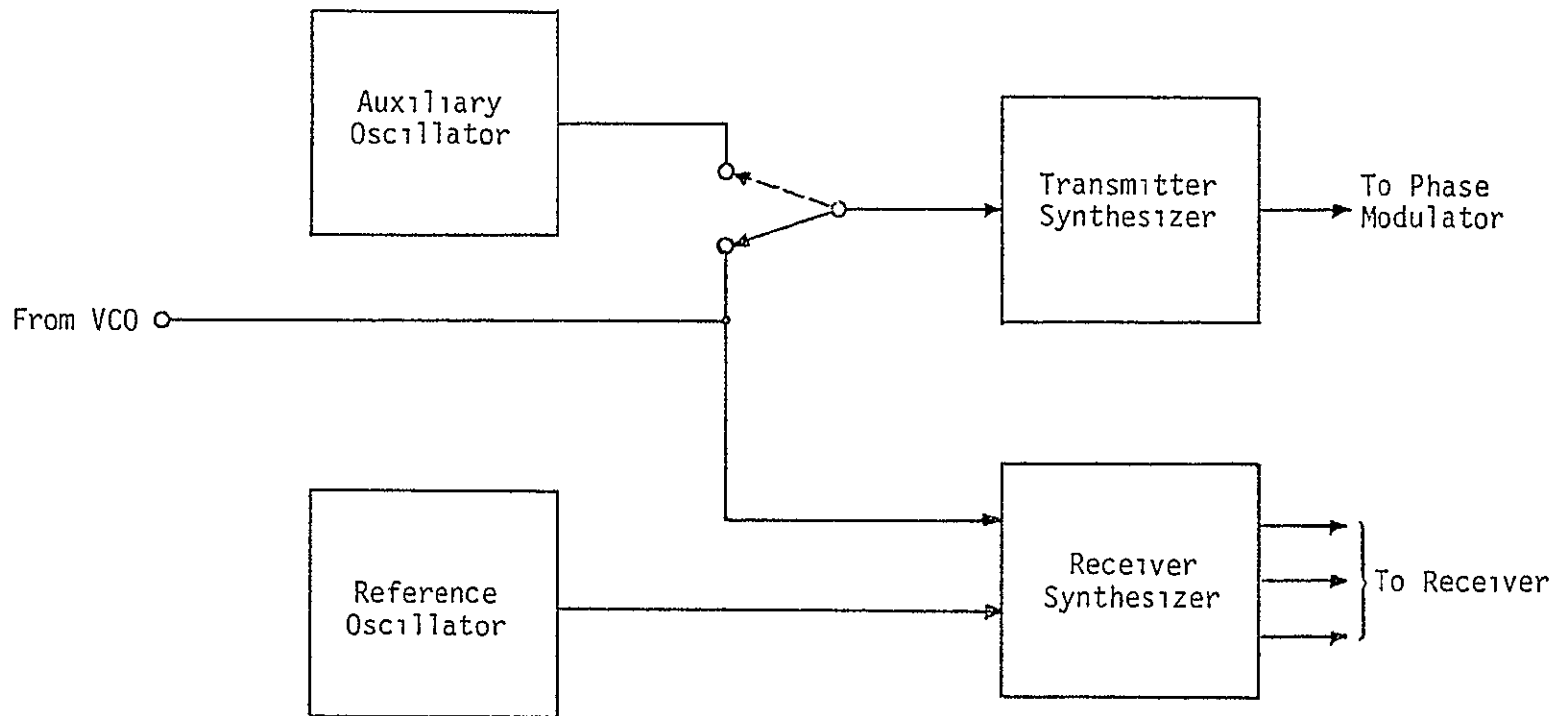


Figure 2-5. PS Synthesizer/Exciter

The transmitter frequency synthesizer multiplies its frequency input to that required by the phase modulator. Input frequency is derived from either the receiver VCO when the receiver is locked or the auxiliary oscillator when the receiver is out of lock.

For NASA transponders, the transmitted S-band to received S-band frequency ratio is 240/221, and for SGLS transponders, the transmitted S-band to received L-band frequency ratio is 256/205.

2.2.3 Phase Modulator

The phase modulator provides the means of modulating the return link carrier with telemetry and ranging signals. Modulation may be supplied from the PS telemetry modulators (2.4) or from any other appropriate source. Input signal frequency response is 0 Hz to 3 MHz and effective carrier phase deviation is linear with input signal voltage over a range of modulation index up to 2.5 radians peak.

2.2.4 Power Amplifier (Figure 2-6)

The output of the phase modulator drives the transmitter frequency multiplier, producing the required modulated carrier signal in the S-band frequency range. Driver output power is 0.2 watts, and the nominal built-in power amplifier is capable of delivering up to 2 watts output. Optional power amplifiers (not an integral part of the PS) may be connected in place of the built-in power amplifier, as needed.

2.3 Command Detector Unit (Figure 2-7)

The CDU consists of two distinct command detector capabilities, one for NASA command signals and one for SGLS signals.

2.3.1 NASA CDU

NASA command data is biphase modulated onto a 16 kHz subcarrier. The subcarrier demodulator functions to regulate the input signal plus noise amplitude and to demodulate the command bits from the subcarrier. A data-aided type suppressed subcarrier tracking loop is employed.

The bit synchronizer is of the digital-data transition tracking loop class and provides accurate bit clock timing to the bit detector. Basically an integrate-and-dump type matched filter, the bit detector serves to maximize the signal-to-noise ratio of the noisy input and to make hard "1" and "0" decisions on the received bit stream.

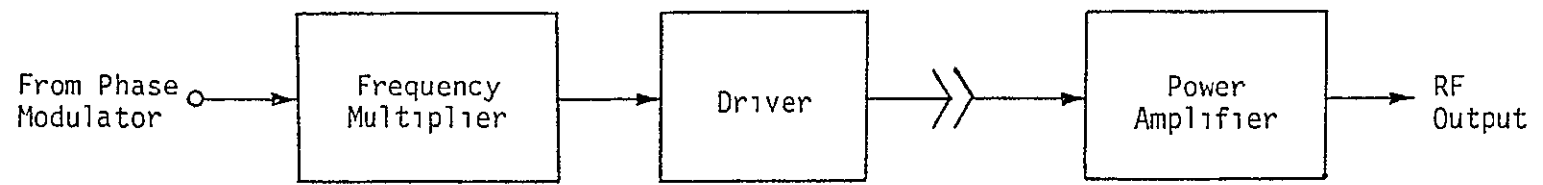


Figure 2-6 PS Power Amplifier

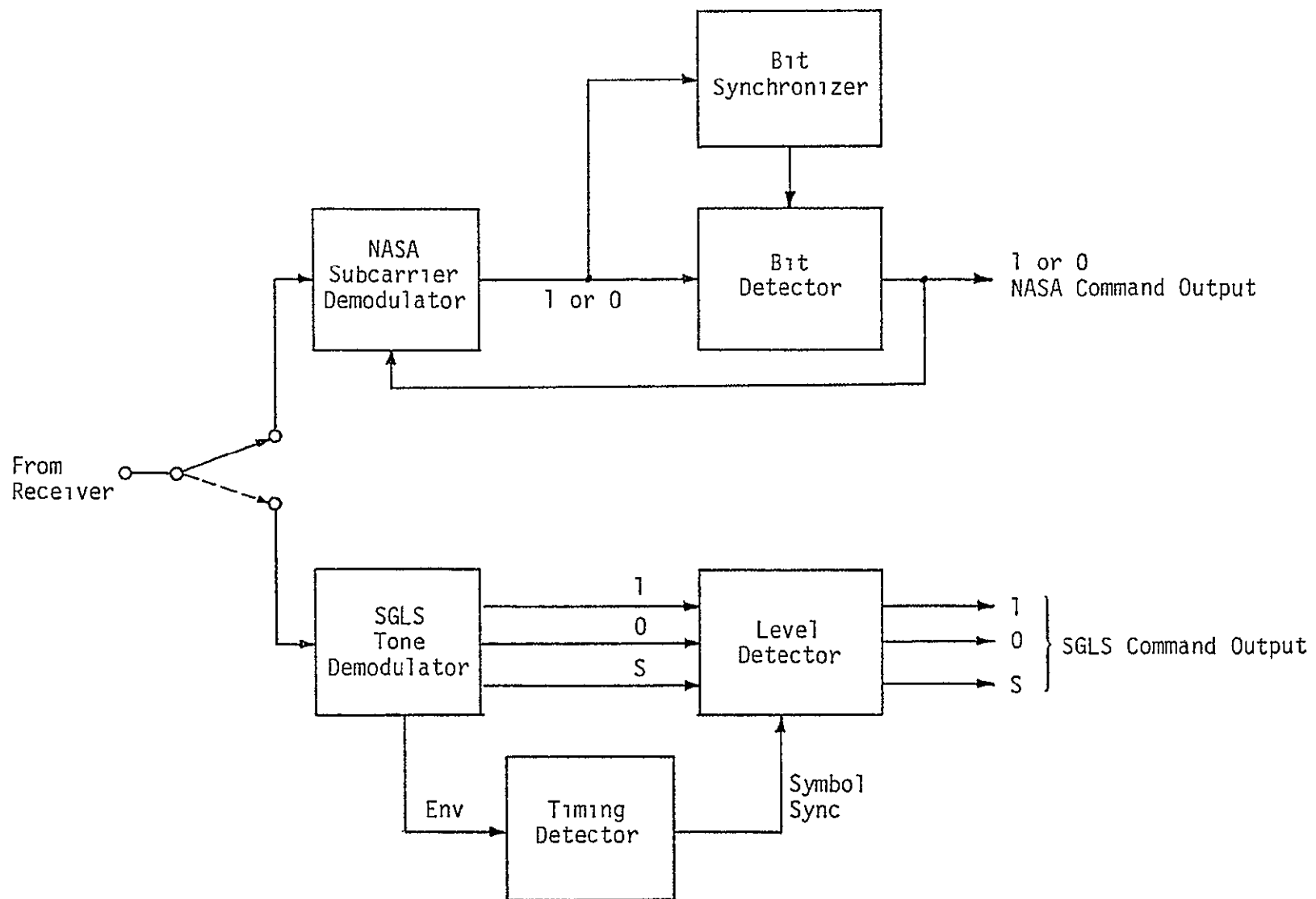


Figure 2-7. PS Command Detectors

The subcarrier demodulator and bit synchronizer contain a lock detection function, which is used to validate the detected command bit sequence. Signal-to-noise ratio information is also generated within the bit detector.

The actual payload flight hardware version of the NASA CDU is standard to all NASA transponders (NE, DS, and TDRSS) and is implemented by means of a sampled data algorithm (sampling at the subcarrier frequency). It is fabricated by means of custom LSI circuits.

Major NASA command parameters are indicated in Table 2-4.

Table 2-4 NASA CDU Parameters

Subcarrier Frequency	16 kHz, sinewave
Bit Rates	2000 - 2^N bps, $N = 0, 1, 2, \dots, 8$
E_b/N_0 for $P_e^b = 1 \times 10^{-5}$	11 dB
Acquisition Sequence	132 bits of alternating 1's and 0's

2 3 2 SGLS CDU

The SGLS command data is ternary in nature. "1," "0," or "S" symbols are transmitted in an MFSK manner, each having a discrete subcarrier frequency or tone. Data rate clock (at one-half the symbol rate) in the form of a triangular signal is amplitude modulated onto the tones.

The tone demodulator consists of three bandpass filter/envelope demodulation channels, each centered on one of the symbol tones. Level detection is made by lowpass filtering the demodulator outputs, sampling the LPFs at the proper time, and making a maximum-likelihood decision as to which of the ternary states is being received.

Timing for the level detector is obtained by recovering the 1/2 symbol rate AM from the composite tones and detecting its zero crossings. In addition, the amplitude of the AM signal is compared with a threshold to produce a squelch indication which activates/deactivates the command output as a function of signal strength.

Major SGLS command parameters are indicated in Table 2-5.

Table 2-5. SGLS CDU Parameters

Signal Tone Frequencies	65 kHz, 76 kHz, 95 kHz
Symbol Rates	1000 or 2000 symbols/second
E_s/N_0 for $P_e^S = 1 \times 10^{-5}$	20 dB

* E_s has a tone component and rate waveform component.
See Appendix D

2.3.3 Command Decoding

No command decoding capability is required within the PS, i.e., no recognition of command address or contents/magnitude will be made. The output of the CDU is handled only on a per-bit basis for input to the support serial-to-parallel data converter (2.6).

2.4 Telemetry Modulators (Figure 2-8)

Two different telemetry modulators are provided; one is a PCM/PSK subcarrier type and the other is a subcarrier frequency modulator.

2.4.1 PCM/PSK Modulator

All NASA and most SGLS normal mode telemetry is transmitted via a biphase modulated 1.024 MHz sinewave subcarrier and high rate SGLS data using a 1.7 MHz subcarrier. The output of the biphase modulator is summed with the ranging signal supplied from the receiver (2.2.1). All signals may be switched in or out as required. The biphase modulated subcarriers and ranging signal amplitudes are independently adjustable at the phase modulator (2.2.3).

Table 2-6 indicates the major PCM/PSK modulator parameters.

Table 2-6. PCM/PSK Modulator Parameters

Item	Parameter/Range
Subcarrier Frequency	1.024 MHz or 1.7 MHz
NASA Bit Rates	16, 8, 4, 2, 1 kbps
SGLS Bit Rates	256,* 128,* 64, 32, 16, 10, 8, 4, 2, 1, 0.5, 0.25 kbps

* 1.7 MHz subcarrier only

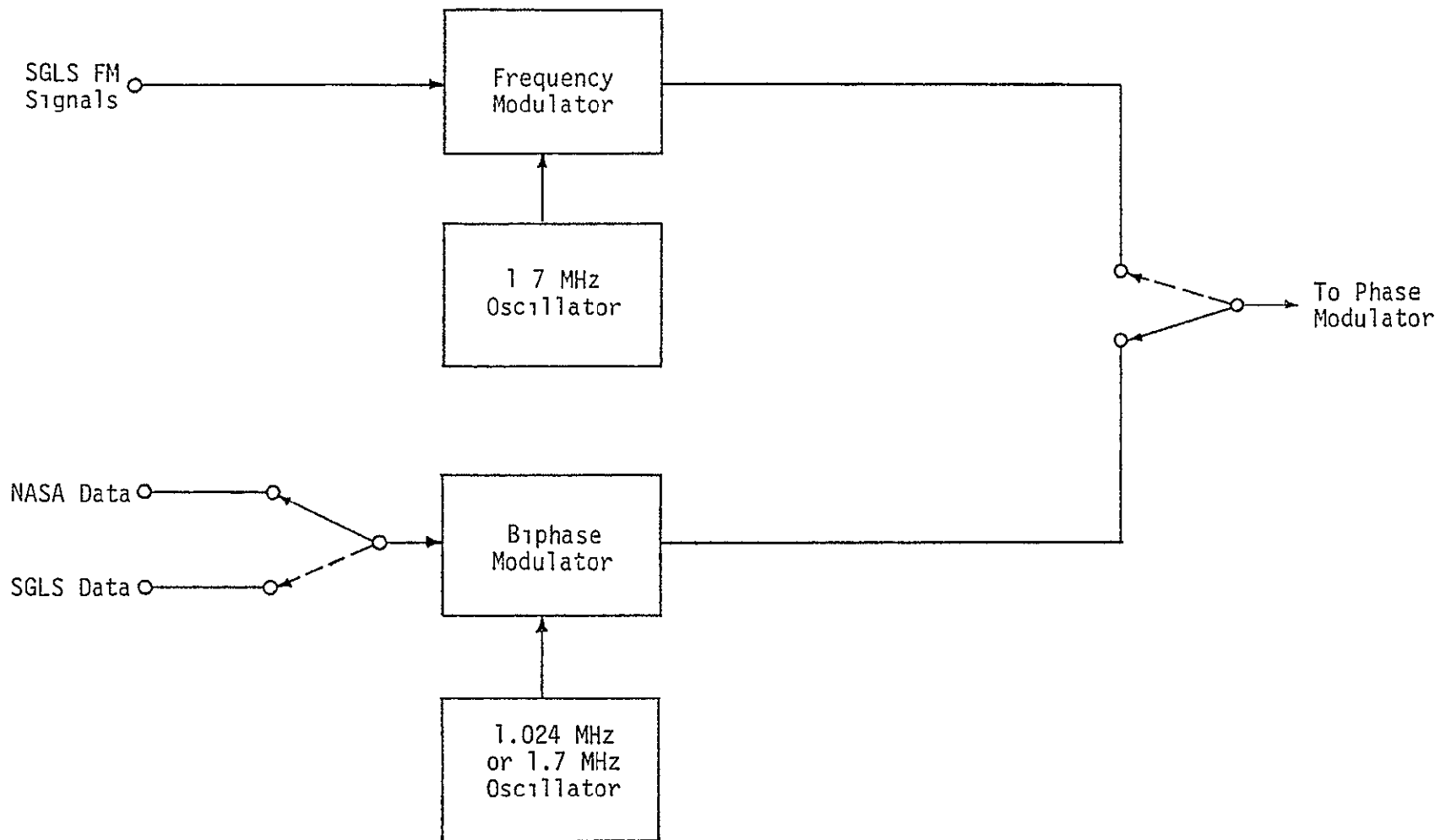


Figure 2-8. PS Telemetry Modulators

2.4.2 Subcarrier Frequency Modulator

This capability is required by SGLS systems and the received signal out of the PI can only be handled by the CIU

The subcarrier frequency is frequency-modulated by the baseband telemetry signals, which consist of either PAM/FM digital data or FM/FM IRIG formats (21 channels).

Subcarrier frequency is nominally 1.7 MHz and maximum deviation is ± 160 kHz.

2.5 Payload Data Processing and Generation

2.5.1 High Rate Data Generator

The high rate data generator is capable of generating serial data streams to bit rates up to 50 Mbps, comprised of (1) pseudorandom bits and (2) structured repetitive formats. The pseudorandom streams may be generated by means of a maximum-length shift register. Structured data is programmable within certain block lengths. The structured data formats are driven by requirements to simulate Spacelab bent-pipe data streams to the Ku-band processor.

2.5.2 Command and Telemetry Multiplexer

The function of the command and telemetry multiplexer is to inject the command data recovered by the payload CDU into the telemetry stream delivered to the Orbiter.

To perform its function, the multiplexer accepts two inputs: (1) simulated telemetry data and (2) detected command data from the CDU. The multiplexer, after proper buffering, then interleaves the replica of the received command with other telemetry information, forming a telemetry frame.

2.6 Data Format Converters/Computer Interfaces

The ESTL Univac 642B computer is used to generate, receive, and compare digital data. Specifically, the computer will:

- (1) Generate NASA pseudorandom and NASA and SGLS fixed format command bit streams
- (2) Receive NASA and SGLS command data from the PS CDU
- (3) Receive NASA telemetry data from the PSP.

- (4) Receive SGLS telemetry from the CIU
- (5) Internally compare generated and received pseudorandom fixed telemetry and command data to determine error rates and patterns

The computer outputs and receives digital data on parallel lines as blocks of bits. Since the input/output interfaces with the PS and ESTL equipment comprise serial data, parallel-to-serial (P/S) and serial-to-parallel (S/P) converters are required. The interface converter units are a part of the payload simulators, although physically they will be located near the computer rather than in the PS cabinet.

The converter that transmits data to the PSP unit (642B/PSP interface) accepts the simulated commands from the computer in the parallel format and then transmits them in a burst serial format to the PSP. The parallel interface also permits the computer to control the PSP configuration.

Serial data output by the PS CDU or the ESTL PSP or CIU is converted from serial to parallel format by the CDU/PSP/642B Interface Unit.

2.7 Special Test Capability

2.7.1 Sampled-Data Monitoring

Sampled-data computational algorithms can provide the means for calibrating and monitoring various important performance parameters. Carrier signal-to-noise ratio may be easily calculated from regular samples taken from the receiver coherent AGC voltage. Carrier suppression can also be determined from the same samples when the receiver input signal is strong. Other vital parameters in the PS may be obtained in a similar manner.

In order to perform the above computations, microprocessors or a minicomputer are required. See Appendix C for a detailed discussion.

3.0 SIMULATOR TEST REQUIREMENTS AND CAPABILITIES

3.1 Task 501 Test Requirements

The prime objective of the Task 501 Program is to verify by test the various RF links that comprise the Shuttle Communications and Tracking System.

Of the many links described in the NASA Task 501 Program Plan (Document EE 7-74-003, June 1974), only detached payload testing is the concern of the PS. Detached payloads are herein defined to include:

- IUS
- NASA near-earth spacecraft
- NASA deep-space spacecraft
- USAF satellites (especially those to be placed into orbits by the IUS)

Primarily, these payloads communicate with the Orbiter PI within a range of 20 miles from the Shuttle for the purpose of Shuttle bay release/deployment checkout prior to execution of their deployed mission operations.

These same payloads are also subject to checkout in the attached configuration (i.e., stowed within the Shuttle bay), where communications may take place via both the RF link and the hardware umbilical cables. The Spacelab is included within the scope of possible payloads in the attached configuration.

The interfaces between the PS and the Shuttle communication equipment (avionics) are limited to the PI, the PSP, and the Ku-band processor. Insofar as the Task 501 tests are concerned, the PI/PSP is the focus of attention.

3.2 Payload Simulator Test Program Objectives

The PS will be used to conduct end-to-end space communications systems compatibility and performance evaluations tests. These tests will be conducted in two phases: Phase I, where the PS is used to evaluate developmental/prototype avionic subsystems in terms of function and overall signal compatibility, and Phase II, where the PS is used in conjunction with the avionic subsystems and selected actual payload hardware (as needed) to accomplish system performance verifications testing.

The goals of both the Phase I and Phase II tests are:

1. To establish equipment/subsystem electrical compatibility.
2. To identify performance and operational limitations and constraints.
3. To verify that appropriate RF and hardwire interfaces are commensurate with mission communications requirements.
4. To verify experimentally that the Shuttle/payload forward and return RF links are signal compatible in all modes.
5. To verify experimentally those tracking, ranging, command, and telemetry channel performance characteristics required for operational mission support.
6. To provide performance data to payload cognizant agencies as an aid to payload communication system development and mission profile predictions

3.3 System Testing With the Payload Simulator

Tests may be classified under two different types:

1. Calibration Tests. Those tests required to establish equipment and performance apart from its operational use. These tests generally establish why the piece of hardware performs in a certain manner. They parameterize the overall or end-to-end performance.
2. Operational Tests. Those tests conducted to measure the equipment performance in terms of its intended use. Such tests establish the input/output and interactive capabilities of the hardware, without specific regard to internal mechanisms.

The PS will undergo calibration tests, act to aid in the calibration testing of other equipment, and become an integral part of the end-to-end systems upon which operational tests are conducted.

Calibration tests will include measurements to establish.

1. Impedances/load characteristics
2. Voltage levels
3. Waveform characteristics
4. VSWR
5. RF power levels

6. Frequency and phase responses
7. Spectra (normal and spurious)
8. Linearity and dynamic range
9. Sensitivities
10. Gains and losses
11. Noise figure
12. Intermodulation products
13. Loop parameters
14. Suppression factors
15. Frequency stability

Operational tests will be conducted to measure:

1. Acquisition characteristics/time
2. Carrier tracking loop performance
 - (a) Transient response
 - (b) Noise threshold
3. AGC performance
4. Lock detector SNR performance
5. Demodulation SNR
6. Turn-around noise
 - (a) Modulation
 - (b) Random
7. Ranging performance
8. Bit error rate
9. Data loss statistics.

The PS embodies two major subsystems—a transponder and a command detector. The transponder may be divided into two subsystems—the RF/IF/demodulator and the modulator/power amplifier. The command detector is partitioned into the subcarrier demodulator and bit detector/synchronizer.

The Shuttle PI may also be subdivided into the modulator/amplifier and RF/IF/demodulator subsystems, while the PSP comprises the subcarrier modulator and subcarrier demodulator and data detector. Figure 3-1 shows the general configuration that will be used for all calibration and performance tests.

Table 3-1 documents the various tests that are to be performed on subsystems and functional configurations. The type of test is also

indicated. Some tests are so routinely conducted they may be classed as both operational and calibration.

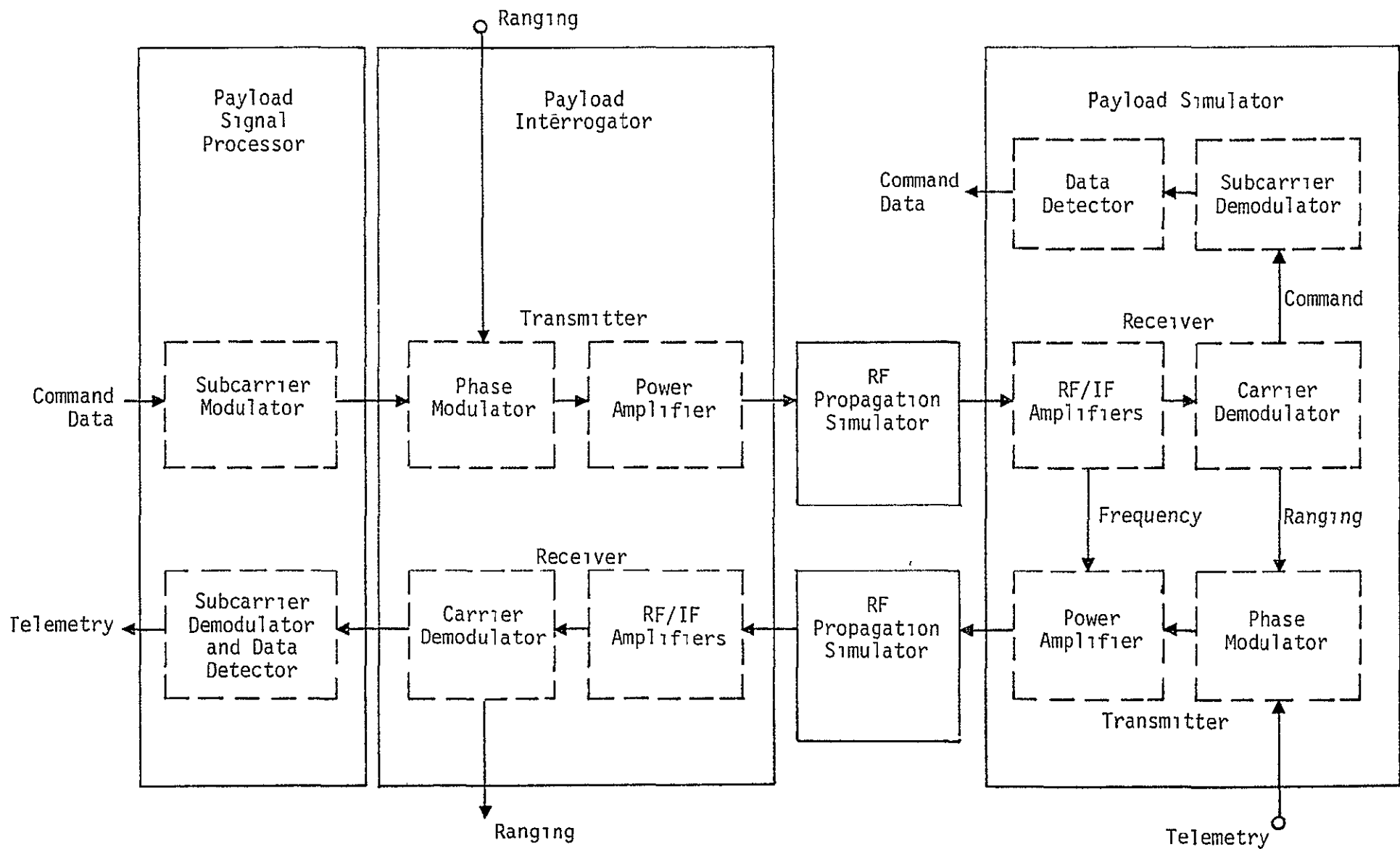


Figure 3-1 General Test Configuration

Table 3-1. Test Summary

Test	Type	
	Operational	Calibration
<u>PS Receiver</u>		
1. Tracking and AGC Loop Parameters		X
2. Noise Figure	X	X
3. AGC vs. Signal Level	X	X
4. Strong Signal Phase Noise	X	X
5. Tracking Loop Noise Biasing		X
6. Frequency Swept Acquisition	X	
7. Absolute Threshold Tracking		X
8. Minimum Operating Point Tracking	X	
9. Lock Detector Statistics	X	X
<u>Command Detection</u>		
1. Detector/Synchronizer Noise/BER		X
2. Subcarrier Demodulation/Detection/ Synchronizer Noise/BER		X
3. CDU Lock Statistics	X	X
4. Complete Forward Link Noise/BER	X	X
<u>PS Modulator/Exciter</u>		
1. Forward Link Modulation Feedthrough		X
2. Modulation Transfer Characteristics		X
3. Modulated Subcarrier Spectra		X
4. Intermodulation Products		X
<u>PI Receiver</u>		
1. AGC vs. Signal Level	X	X
2. Strong Signal Phase Noise	X	X
3. Frequency Acquisition	X	
4. Absolute Threshold Tracking		X
5. Minimum Operating Point Tracking	X	X
6. Lock Detector Statistics	X	X
7. Forward Link Threshold Effects	X	
<u>Telemetry Detection</u>		
1. Intermodulation Effects		X
2. PCM/PSK/PM Noise/BER	X	
3. FM/PM Noise/BER	X	
<u>Ranging</u>		
1. Two-Way Ranging Tone Delay		X
2. Two-Way Ranging Tone Relative Phase Shift		X
3. Intermodulation Effects		X
4. Complete Ranging Performance	X	

4.0 DETAILED SIMULATOR HARDWARE DEFINITION

This entire section of the report is intended to provide detailed information on the performance, design, and operation of each of the PS subsystems.

The design philosophy and approach are based upon tradeoff studies which have considered function, flexibility, operating factors, change/growth, operating environment, and cost minimization. For the sake of brevity, most tradeoffs are not given detailed discussion in this report. The designs presented are those which Axiomatix believes best meet the PS requirements and represent sound engineering practice and experience.

In the Detailed Implementation subsections, various hardware approaches, values, and manufacturers' model numbers are stated. These details have been supplied to facilitate the design description and to give a basis for realistic costing. Thus, these details must be considered as representative or typical, although Axiomatix believes they adequately and properly satisfy all specifications at the present level of development.

4.1 Transponder

4.1.1 General Description

The transponder consists of two distinct signal processing functions: (1) a receiver which accepts very weak RF signals and acts to amplify and detect them and (2) a transmitter which generates strong RF signals for transmission.

The transmitter frequency is related to the receiver frequency by the ratio of integers, called the coherency ratio. The NASA receive frequency range is S-band (2025 to 2120 MHz), while the SGLS receive frequency range is L-band (1760 to 1840 MHz). Both the NASA and SGLS transmitter frequency ranges are S-band (2200 to 2300 MHz). The corresponding coherency ratios are, for NASA, 240/221, and for SGLS, 256/205.

The output of the transponder receiver is the command signal and lock indication, while the input to the transmitter is the telemetry data. In addition, a ranging signal (tone set) is "turned-around" from the receiver to the transmitter.

4.1.2 Generic Description

Figure 4-1 shows a generic block diagram of the payload simulator transponder

The RF input is first passed through a pre-selector (bandpass filter) which encompasses either the S-band or L-band receiver frequency ranges. Next, the received frequency, f_{in} , is mixed with the first local reference, f_1 , to produce the first intermediate frequency, f_{I1} . The first IF amplifier is voltage-gain controllable such that, by means of an automatic gain control (AGC) voltage, the subsequent stages will be operated in their linear regions.

The first IF output, f_{I1} , is next mixed with the local reference frequency, f_2 , resulting in the second IF, f_{I2} , which is equal to the receiver reference frequency, f_R ($f_{I2} = f_R$). This second IF signal is then channeled to four demodulators as shown in Figure 4-1.

The tracking demodulator produces a phase error signal which is input to the carrier voltage controlled oscillator (VCO). Mixed with the reference oscillator frequency in the frequency synthesizer, the VCO output produces the coherent references f_1 and f_2 . The net result is that any receiver phase error is automatically driven to zero.

Command, AGC/lock, and ranging signals are produced by the other three demodulators.

The frequency synthesizer also generates the coherent frequency, f_A , which is input to the transmitter chain. This frequency is first multiplied by an integer to produce the phase modulator excitation frequency, f_B . The phase modulator accepts the telemetry and ranging base-band signals and phase modulates them onto the carrier at frequency f_B . In turn, the phase modulator output is multiplied by a second integer to obtain the transmitter output frequency, f , along with the proper telemetry and ranging phase modulation indices.

The exciter amplifies the transmitter signal to a lower power level (approximately 23 dBm), and the power amplifier increases it to a 10 dB higher power level (approximately 33 dBm). The transmitter output may be taken from either the exciter or power amplifier outputs, depending upon the application.

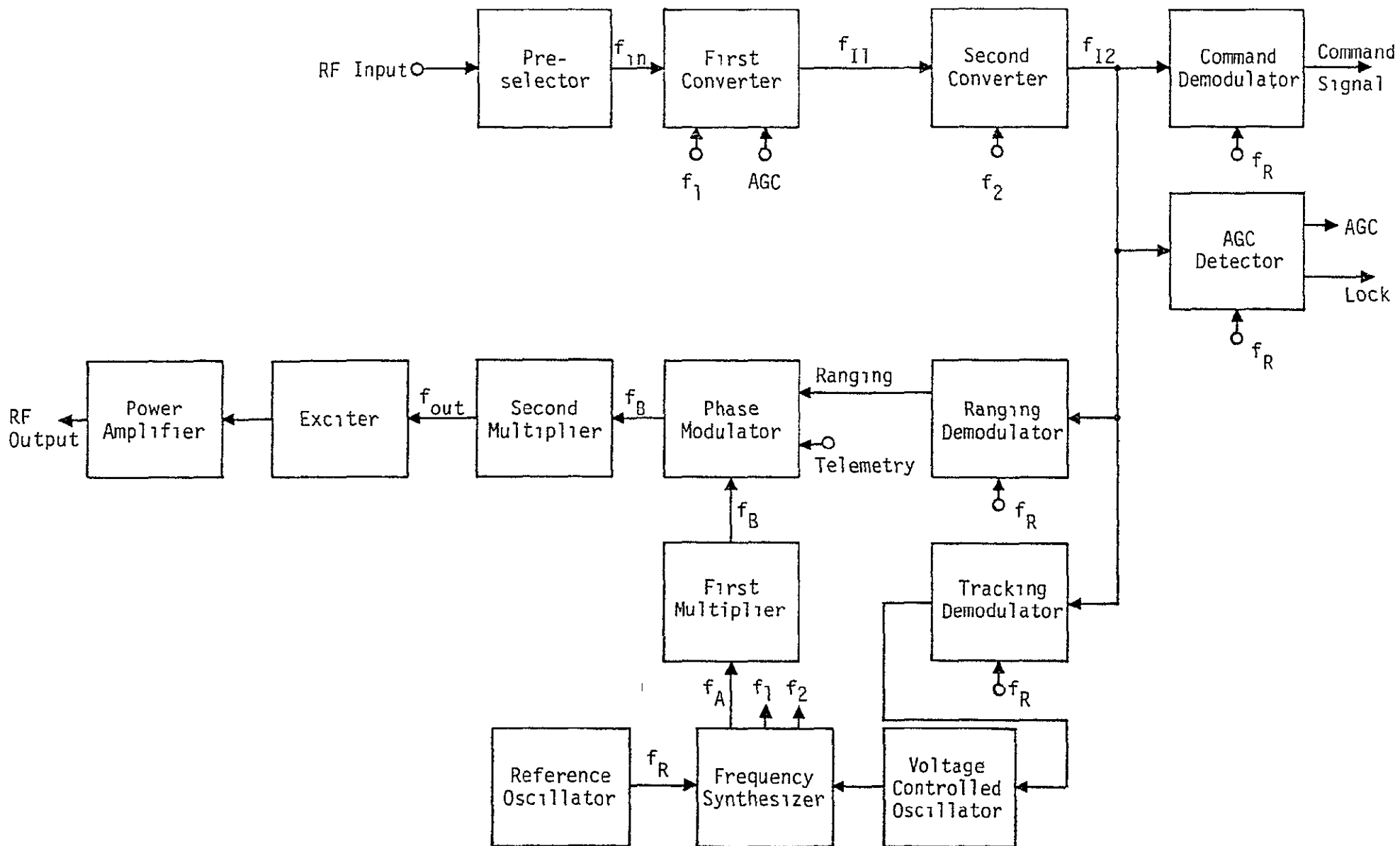


Figure 4-1. Simulator Transponder Generic Block Diagram

4.1.3 Functional Description

Two fundamental approaches may be taken to realize the transponder: (1) design an entirely new (from scratch) transponder to meet the requirements or (2) adapt existing transponder designs to provide the requisite functions. In view of a large number of existing, well proven transponder designs, coupled with a requirement for low cost, a new transponder design rapidly appears unjustified.

The following flight transponders and ground receivers were considered as candidate existing designs upon which the PS transponder might be based.

Flight Transponders

- 1 NASA Standard Near Earth Transponder
2. NASA Standard Deep Space Transponder
- 3 Shuttle S-Band Transponder
- 4 IUS Transponder
5. SGLS Transponder

Ground Receivers

1. STDN Multifunction Receiver (MFR)
- 2 DSN Block-IV Receiver
- 3 STDN Test Receiver

All of the flight transponders use the same fundamental architecture, differences are manifested in terms of sensitivity, input frequency range, tracking bandwidths, ranging characteristics, and output signal characteristics. These differences are, however, not gross, and all of the transponders listed exhibit similar performance.

There is more disparity between the ground receivers, not in terms of performance as measured from input/output characteristics, but in terms of the internal architecture such as IF frequencies, reference frequency synthesis, loop length, and various acquisition and tracking features. In addition, these receivers are not transponders; thus, they have no transmitter capability.

A comparison was made between the general payload transponder (PT) architecture and what was considered to be the most representative ground receiver (in terms of architecture), the MFR. The advantages and disadvantages of the two fundamental approaches are as follows.

PT ArchitectureMFR Architecture

ADVANTAGES

- | | |
|--|---|
| <ol style="list-style-type: none"> 1. Provides an analogous emulation of actual payload transponder receivers in terms of the heterodyne operations. 2. Some circuits may be copied or modified versions of actual flight transponder circuits | <ol style="list-style-type: none"> 1. Current designs may be largely employed with little or no modification 2. Performance and limitations are well established and documented. 3. Probably lower cost modules and assemblies than the PT architecture due to existing design, especially if surplus assemblies are available |
|--|---|

DISADVANTAGES

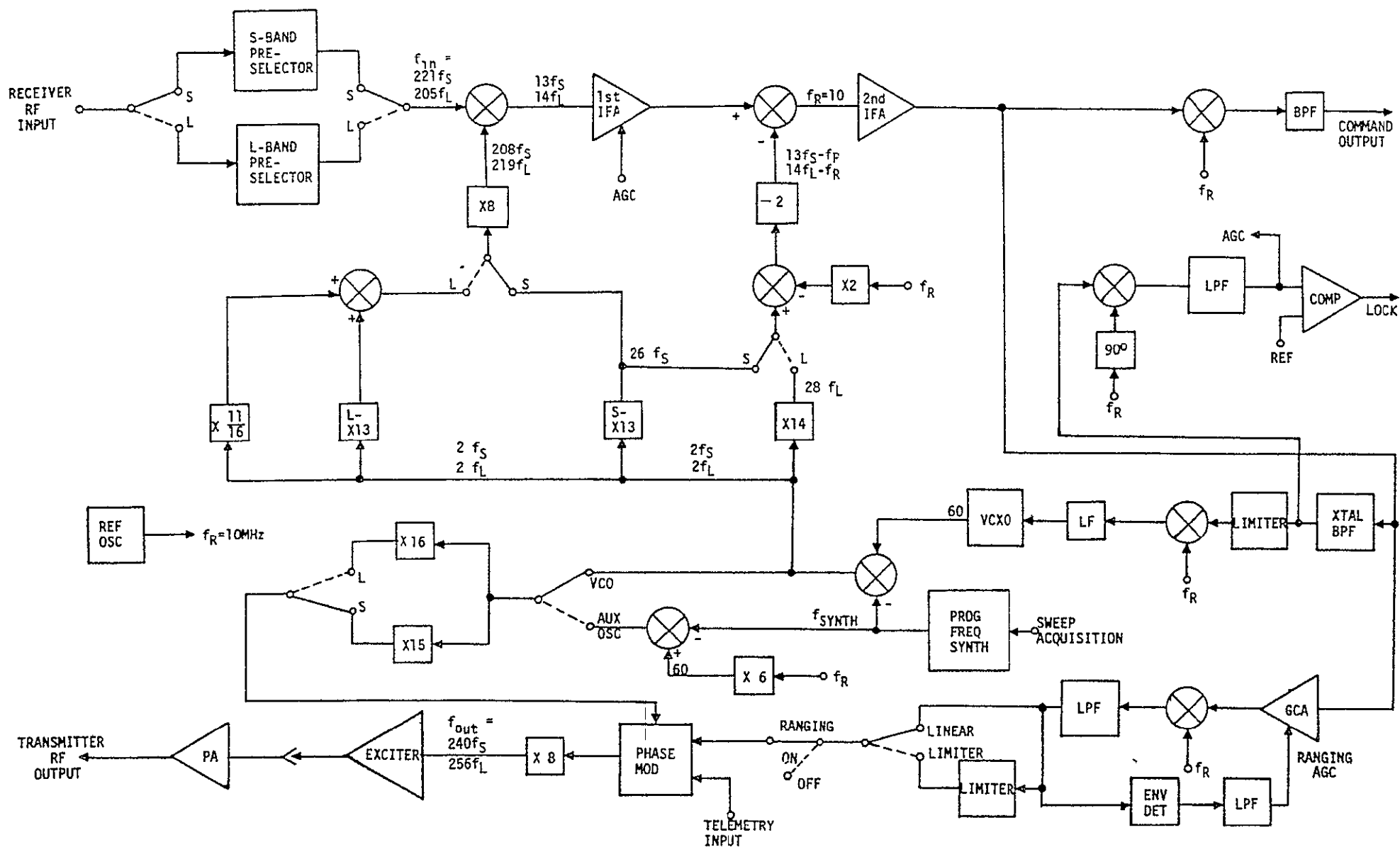
- | | |
|---|--|
| <ol style="list-style-type: none"> 1. Circuits which are not derived from existing flight transponder circuits will have to be procured, or designed and fabricated. 2. Performance may vary as a function of input frequency due to frequency dependent circuits that are not perfectly "aligned" to each input frequency. | <ol style="list-style-type: none"> 1. Architecture is different from that of the payload flight transponders. A functional relationship exists only in terms of input/output functions, but not necessarily in terms of all transfer characteristics 2. A complete MFR has many features and capabilities that would not be used for the payload simulator. If a complete MFR must be procured for the simulator, its total cost, relative to the portions that would actually be used, is probably unjustified 3. Has no companion coherent transmitter. |
|---|--|

In the opinion of AXIOMATIX, the PT architecture advantages/disadvantages relative to those of the MFR dictate that the PT architecture should be used for the PS. This approach was therefore selected and is functionally described in the following paragraphs.

A functional block diagram of the payload simulator transponder appears in Figure 4-2. The major functions, along with their descriptive specifications, are detailed in the following sections

4.1.3 1 Pre-Selectors and First Mixer

The pre-selectors are broadband bandpass filters which function



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Figure 4-2. Payload Simulator Transponder Functional Block Diagram

to. (1) match the input signal cable/antenna to the first mixer, and (2) provide attenuation at the mixer image frequencies ($195f_S$ and $233f_L$). The bandwidth of the pre-selectors is sufficiently wide to cause no more than 0.5 dB of relative attenuation across the range of S-band and L-band input frequencies.

The two input frequency bands are designated in terms of their basic coherency frequencies, f_S (S-band) and f_L (L-band). Receiver mixer frequencies are also functions of the coherency frequencies. Nominal (mid-band) values are $f_S = 9.38$ MHz and $f_L = 8.78$ MHz.

The receiver frequency scheme has been structured to allow a single IF chain to be used for both S-band and L-band inputs and as many common mixer frequency circuits as possible. Thus, the first mixer reference and output frequencies for S-band and L-band are similar, e.g., the nominal values are:

$$\begin{aligned} 208 f_S &= 1951 \text{ MHz} \approx 219 f_L = 1923 \text{ MHz} \\ 13 f_S &= 122 \text{ MHz} \approx 14 f_L = 123 \text{ MHz} . \end{aligned}$$

Note that, for S-band, the first mixer reference frequency is below the input frequency while, for L-band, it is above. Also note that the first IF is not a fixed frequency (as is the case for some receivers) but changes with the input frequency. This approach is consistent with NASA and SGLS receiver architectures (It is exact for NASA, and approximate for SGLS by virtue of the use of a common IF as explained above.)

4.1.3.2 IF Amplifiers and Second Mixer

The first IF amplifier (IFA) is gain controllable by means of a reference voltage. An automatic gain control (AGC) voltage is generated in a detector operating on the residual carrier component (see Section 4.1.3.5) and used to regulate the output of the first IFA to a constant carrier power level. The dynamic range is 100 dB.

The second mixer has a constant frequency output (independent of the receiver coherency frequency) of 10 MHz. The 10 MHz frequency is defined to be the receiver reference frequency, f_R . Second mixer frequencies are either $13f_S - f_R$ or $14f_L - f_R$. The second IFA has a fixed gain, and its output is distributed to the four baseband demodulators (phase-detectors).

4.1 3.3 Mixer Reference Frequency Synthesis

Underlying the frequency synthesis are the frequencies $2f_S$ and $2f_L$. These are produced by mixing the receiver voltage controlled crystal oscillator (VCXO) output (60 MHz nominal) with a frequency produced from a programmable frequency synthesizer. The programmable frequency synthesizer is set to produce the proper value of f_S or f_L according to the following relationships:

$$f_{\text{synth}} = \begin{cases} 60 - 2f_S = 60 - f_{\text{in}}/110.5 \\ 60 - 2f_L = 60 - f_{\text{in}}/102.5. \end{cases}$$

Table 4-1 lists the range of f_{synth} .

Table 4-1. Programmable Synthesizer and First IF Frequencies

	Receiver Input Frequency f_{in} (MHz)	First IF (MHz)*	Programmable Synthesizer f_{synth} (MHz)*
S-Band	2120 (maximum)	$13 f_S = 124.7$	40.81
	2072 (mean)	$13 f_S = 121.9$	41.24
	2025 (minimum)	$13 f_S = 119.1$	41.67
L-Band	1840 (maximum)	$14 f_L = 125.7$	42.05
	1800 (mean)	$14 f_L = 122.9$	42.44
	1760 (minimum)	$14 f_L = 120.2$	42.83

*Values are rounded.

To obtain the first mixer frequencies, $2f_S$ is frequency multiplied by 13 and then by 8 to generate $208f_S$, and $2f_L$ is multiplied by 219/16 and by 8 to derive $219f_L$. Second mixer frequencies are derived by mixing $26f_S$ and $28f_L$ with $2f_R$, and then dividing the difference frequency by 2. (NOTE: f_R is supplied by a stable, fixed frequency reference oscillator.)

4.1.3 4 Command Demodulator

The command demodulator consists of a phase detector followed by a BPF. Phase detector reference frequency, f_R , is in phase-quadrature

with the residual carrier component, thus placing it in-phase with the command sidebands. The baseband command signal, which consists of a bi-phase modulated 16 kHz subcarrier for NASA commands or a set of three MFSK tones (65, 76, and 95 kHz) for SGLS commands, is output to the command detector unit (CDU) via the BPF. This filter consists of the cascade of a high-pass filter with 3 dB frequency of 500 Hz and a low-pass filter having a 3 dB frequency of 130 kHz

4.1.3.5 AGC and Lock Demodulator

A phase detector whose reference is in-phase with the residual carrier component produces a direct voltage proportional to the received carrier power level. The reference phase is formed by passing f_R through a 90° phase shift network. A BPF preceding the phase detector allows only the residual carrier component of the received signal spectrum to reach the phase detector

The direct voltage is smoothed by a LPF to remove the large noise variations and is then fed back to the first IFA to complete the AGC loop. In addition, the voltage is compared with a predetermined, fixed reference voltage to establish whether the receiver residual carrier tracking loop is in or out of lock. Since the direct voltage output of the phase detector varies as the cosine of the receiver phase error, it is maximum (and steady) when the receiver is in-lock and is therefore a reliable measure of this condition.

Internal to the receiver, the in-lock indication is used to disable the sweep of the programmable frequency synthesizer when it is employed as a receiver acquisition aid. See Section 4.1.3.6 for further details

Finally, it is noted that there is no effective AGC when the receiver is out-of-lock. This, however, is not a detriment to receiver acquisition, as the tracking loop phase detector is already preceded (by design) with an amplitude limiter; thus, any limiting that might occur in the IFAs due to the absence of AGC will not alter acquisition performance

4.1.3.6 Tracking Demodulator (The PLL)

The tracking phase detector is preceded by a bandpass limiter (BPL). A narrow BPF selects only the discrete carrier component from

the received signal spectrum. This is then passed through an amplitude limiter which produces a hard-clipped (signum-function) version of its input. Finally, another BPF retains only the first-zone (fundamental) output of the limiter, which is then input to the phase detector.

The purpose of the BPL is to provide a known threshold operating point for the phase-locked tracking loop (PLL) when reliable receiver AGC is not attainable. Details of the BPF operation may be found in [4,5].

The carrier phase error produced at the output of the phase detector is filtered by a standard second-order loop filter network and then input to the VCXO. The loop is closed through the frequency synthesis circuits (4.1 3.3) to the IF mixers. Architecture of the receiver PLL is often called the "long-loop" (see [5]). Effective loop-phase-error multiplication factors are 110.5 for S-band and 102.5 for L-band.

As an aid to acquiring the receiver under conditions of large received frequency uncertainty, closed loop swept-frequency acquisition may be employed. This is accomplished by manually setting the programmable frequency synthesizer to its nominal value relative to the expected received frequency and then sweeping the synthesizer linearly above and below its nominal value. The sweep range is a function of the maximum uncertainty, and the sweep rate is determined by the PLL natural frequency and the response time of the receiver lock detector. When lock occurs, as determined by the lock detector, the sweeping action is discontinued. Whether the programmable synthesizer is held at the frequency for which lock was obtained or returned to its nominal frequency is dependent upon operational considerations.

4.1.3.7 Ranging Demodulator

The second IF signal is passed through a gain controlled amplifier (GCA) before being applied to the ranging phase detector. Demodulating by means of the reference frequency f_p , the ranging baseband linear signal is low-pass filtered with a 3 dB frequency of 1.5 MHz.

The LPF output is envelope detected and further filtered to provide a ranging AGC voltage to the GCA. This loop functions to maintain a constant RMS signal-plus-noise level at the output of the ranging demodulator.

Ranging demodulator linear output is also passed through a hard-limiter in order to generate a "square" (two-level) waveform. A selector switch is provided to make either the linear or limited ranging signal available to the transmitter phase modulator. The choice of waveforms is an operational consideration.

4.1 3.8 Transmitter Chain and Phase Modulator

The $2f_S$ and $2f_L$ frequencies, generated as discussed in Section 4.1.3.3, form the VCO input to the transmitter chain. An alternate source of $2f_S$ and $2f_L$ used for transmitter excitation, and designated as the auxiliary oscillator, is formed by mixing the programmable frequency synthesizer output with six times the reference oscillator frequency. A switch selects between the VCO and auxiliary oscillator, depending respectively on whether the receiver tracking loop is in-lock or out-of-lock. Override is also provided to place the switch in either position irrespective of the receiver lock status.

The $2f_S$ frequency is multiplied by 15 to obtain the S-band drive to the phase modulator, and the $2f_L$ frequency is multiplied by 16 to produce the L-band drive. The respective nominal frequencies (mid-band) are 281.4 MHz and 281.0 MHz, or essentially the same frequency. A switch selects the X15 and X16 outputs.

A phase modulator functions to linearly shift the phase of an input sinusoid with respect to the phase-modulating voltage. The underlying principle of operation is a varactor (voltage variable capacitor) controlled phase-shift network. The impressed modulating waveform changes the circuit capacitance so that the input RF sinusoid is linearly phase-shifted about a nominal (zero volt) operating point, depending upon the instantaneous sign and magnitude of the voltage. Due to the frequency X8 circuit which follows the phase modulator, the linear range of the modulator proper need only be 1/8 of the transmitter total linear phase deviation range of ± 2.5 radians.

The output of the X8 multiplier is $240f_S$ or $256f_L$, with the proper phase deviation as established by the telemetry input voltage. The exciter amplifies this signal to the 0.2 watt (+23 dBm) level, at which point the output may be taken for cable connecting links to the payload interrogator. A power amplifier further raises the power level to 2 watts (+33 dBm) for use primarily with air (antenna) links.

4.1.4 Detailed Transponder Implementation

Figure 4-3 shows a detailed block diagram of the transponder. Power levels, gains, and losses are indicated at critical points. The following sections discuss implementation details, tradeoffs, and hardware types.

4.1.4.1 Pre-Selector, First Converter and Input IFA

The pre-selector filters are envisioned to be of the interdigital/compline type. Bandwidths (1 dB) required are 2000-2150 MHz (S-band) and 1700-1900 MHz (L-band). Nominal centerband insertion loss* should not be greater than 2 dB.

The selector switches (if actual switches are used) should be low-leakage, resistive-terminating (to open ports), coaxial-mechanical types. Alternatively, the pre-selectors may be physically mounted (one at a time) to a connector base using N-type connectors. This latter approach will provide the lowest VSWR and leakage but is less operationally convenient and subject to connector damage/wear over a prolonged number of change-outs.

The first mixer is a double-balanced MIC type (RHG DM 1-2, or equivalent), with a noise figure of 7 dB and a conversion loss of 5 dB. Reference frequency level drive is +10 dBm.

The input IFA has a gain of 56 dB and a noise figure of 3.5 dB. For this amplifier, as well as all of the other RF amplifiers shown in Figure 4-3 and discussed in this report, cascadable thin-film units such as those manufactured by Watkins-Johnson or AvanteK are assumed. AvanteK Model UTC5-135 satisfies the input IFA requirement.

Receiver noise figure at the RF input port is calculated according to the following equation:

$$F = F_p + [F_M + (F_A - 1)L_C - 1]L_p,$$

where $F_p = L_p$ is the noise figure or transmission loss of the preselector,
 F_M is the noise figure of the mixer,

* Insertion loss numbers in this report are the anticipated maximums (worst-case) and include connector and interconnecting cable losses.

L_C is the conversion loss of the mixer, and

F_A is the noise figure of the first IFA.

With $F_p = L_p = 2$ (maximum band edge value), $F_M = 5$, $L_C = 3.2$, and $F_A = 2.2$, the input noise figure is $F = 17.68 = 12.5$ dB.

4.1.4.2 First IFA Chain

The output of the input IFA (+56 dB gain) is filtered by a band-pass filter. Center frequency is 122.5 MHz and the 3 dB bandwidth is 30 MHz. A four-section tubular filter (K&L Microwave or AEL Inc.) will adequately serve this function.

A 20 dB directional coupler allows the BPF output to be sampled for the purpose of received signal power monitoring and noise figure determination. (A Merrimac Model CRM-20-225 is a typical coupler.) The coupling port is fed through a variable attenuator to a 47 dB gain amplifier. The amplifier output is supplied external to the receiver as the monitor point. A pair of HP step attenuators, 10 dB/step and 1 dB/step, will allow the monitor point to be set at the desired power level without amplifier overload. The 47 dB amplifier may be an Avantek Model UTC5-132.

The 100 dB VVA is comprised of cascaded PIN-diode Pi-networks, as shown in Figure 4-4. It is estimated that four sections will be required to realize the 100 dB range. The attenuator networks may be constructed from discrete components or obtained as thin-film MICs, e.g., Watkins-Johnson WJ-G1. Since the attenuation (in dB) versus control voltages for these networks is reasonably nonlinear, a linearizer network is required. This may be realized using an operational nonlinear amplifier and implemented via a breakpoint-diode controlled resistor configuration. If uniform (similar attenuation) networks are available, a single linearizer may serve all attenuators; otherwise, individual custom adjusted linearizers are required. The input amplifier to the linearizers should have a gain which matches the external control voltage to the attenuator range. Absolute maximum gain through the attenuator should be about 10 dB, while full attenuation transfer is on the order of -105 dB. The 15 dB amplifiers (Avantek UT0-511) have a 2.5 dB noise figure.

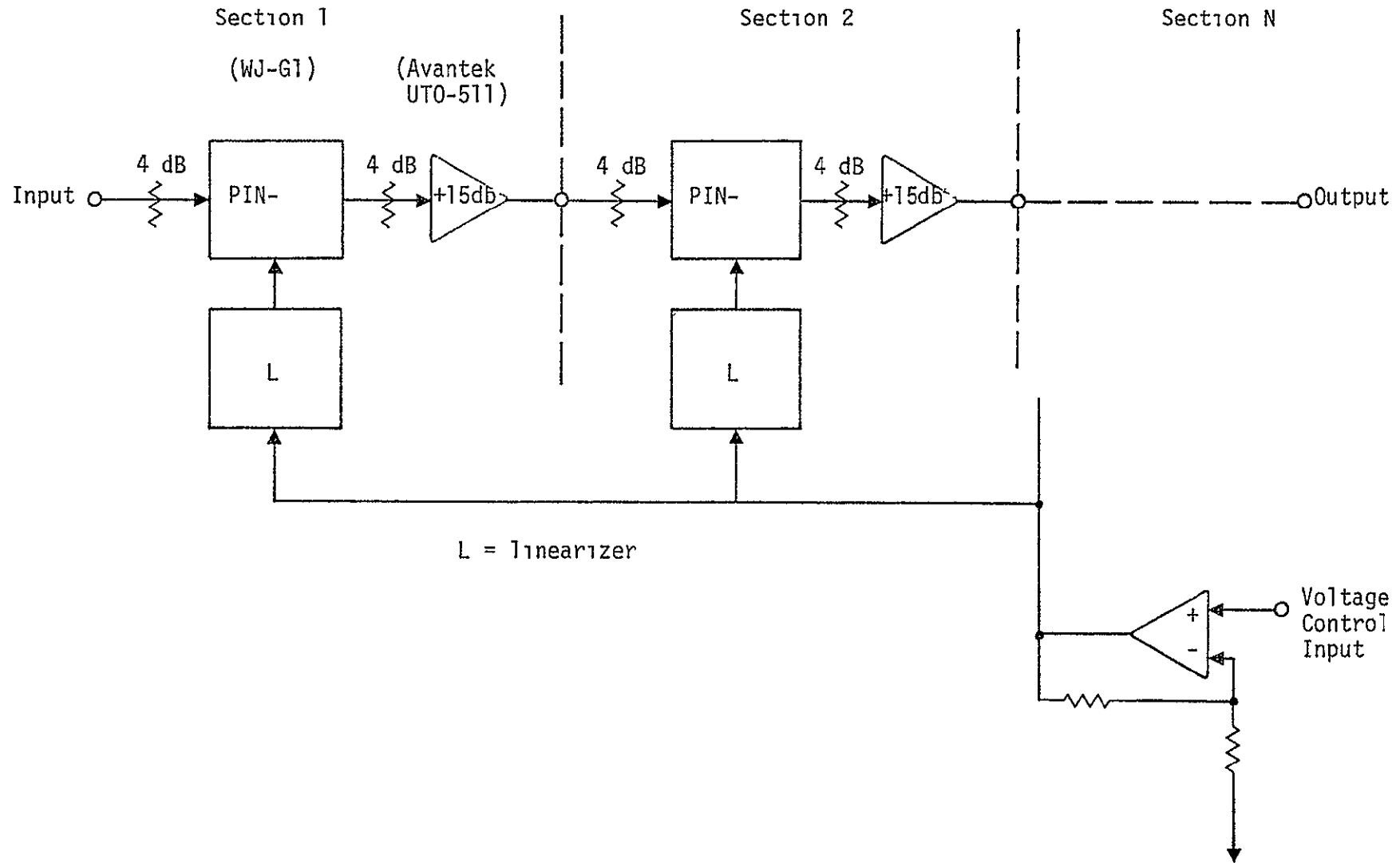


Figure 4-4. Voltage Variable Attenuator

The amplifier between the VVA and the second mixer has a 15 dB gain. A 10 dB pad is inserted between the amplifier output and mixer input.

4.1.4 3 Second Converter and Second IFA Chain

A double-balanced mixer (Merrimac DMM-2-250, or equivalent), operating at a reference drive level of +10 dBm and with a conversion loss of 7 dB, is employed to produce the 10 MHz IF. The 47 dB amplifier is an Avantek UTC-118. A BPF with 5 MHz 3-dB bandwidth is employed between the 57 dB amplifier output and 43 dB amplifier input. This filter is a linear-phase LC type (e.g., Allen Avionics, 50% bandwidth, Gaussian type). The 57 dB amplifier is an Avantek UTC5-127.

A four-way power divider (Merrimac Model PDS-40-17, or equivalent) splits the 10 MHz IF signal for input to the tracking/AGC, ranging, and command channels.

4.1.4.4 10 MHz Narrowband IF Circuits

Two 4-pole crystal filters, with 1 kHz and 10 kHz 3 dB bandwidths, respectively, are used to extract the residual carrier component from the received signal spectrum. The 1 kHz bandwidth is typically used for NASA/DS receivers, while the 10 kHz bandwidth is employed when emulating NASA/NE and SGLS configurations. An operator-controlled switch selects between the narrow and wide positions.

A two-way hybrid (Merrimac PDM-20-10) splits the filtered carrier component into the AGC and tracking channels. The AGC IFA has a 35 dB gain (Avantek UTC5-160), providing a +12 dBm signal level drive to the AGC phase detector. A Watkins-Johnson Model M9E mixer is specified for the phase detector,* and a reference drive level of +23 dBm will be employed.

The tracking channel utilizes an amplitude limiter, the general configuration being shown in Figure 4-5. The number of stages required is that necessary to provide full limiting on the noise voltage from the 1 kHz BPF when there is no signal at the receiver input. Three

* High level phase detectors are specified for all 10 MHz phase detectors (tracking, AGC, command, and ranging), so that large gain dc amplifiers are not required in the baseband output circuits.

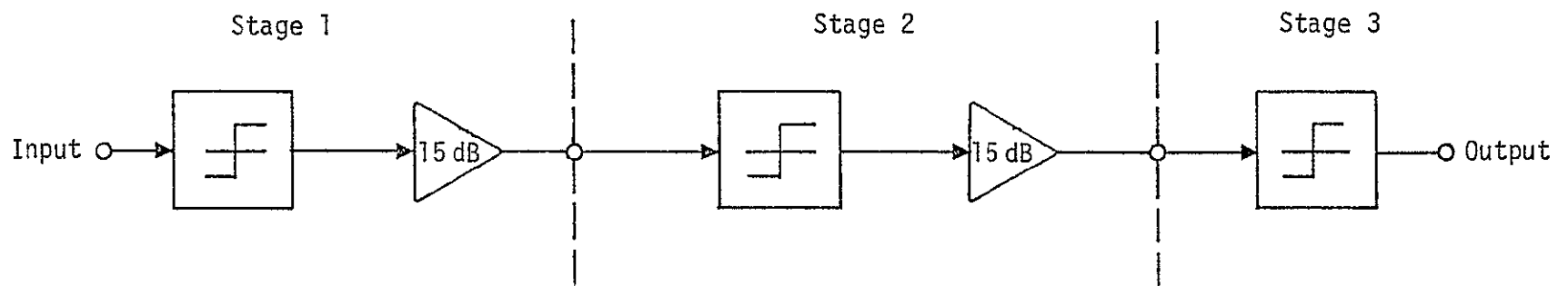


Figure 4-5. Cascade Limiter Circuit

stages of a Watkins-Johnson WJ-L1 limiter followed by a WJ-A7 amplifier, except at the output stage, suffices. An alternative is to use a complete limiter module (e.g., MITEQ Model LMP-1A-10.7).

The 500 kHz bandwidth filter following the limiter is a two-pole LC type and is padded on both the input and output by 6 dB attenuators. Following the filter, the cascade of a WJ-A5 followed by a WJ-A79 provides the proper signal drive level to the tracking phase detector.

4.1.4.5 Tracking Loop Filters

DC amplifiers are required in the PLL filter circuits. For this application, very low input offset voltage/current drifts must be obtained. The first amplifier provides any necessary dc gain so that the PLL open loop gain will meet its design requirement. A lowpass breakpoint is provided at 5 kHz so that additional attenuation of command and ranging sidebands due to crystal filter response sidelobes will be effected.

A good amplifier for implementing the loop voltage gain (G_{DC}) circuit is the Burr-Brown 3291/14 chopper stabilized operational amplifier. The input resistor R_B should be on the order of $1k\Omega$, and $R_B C_B = 31.8 \times 10^{-6}$ sec.

The loop filter (R_1, R_2, C) is a passive second-order type, whose component values may be calculated according to relationships found in [5] as a function of loop natural frequency, damping factor, and gain. Several standard loop bandwidths are to be supplied (e.g., 18, 200, and 1000 Hz) and selected according to the transponder type being simulated.

A voltage follower buffers the loop filter from the VCXO input. The amplifier recommended is Burr-Brown FET Input Model 3521L.

4.1.4.6 Frequency Sources and Receiver Frequency Synthesis

Three independent frequency sources are required. First, there is the 60 MHz crystal voltage controlled oscillator. This unit should have high stability, and a temperature-compensated type is recommended. The deviation sensitivity should be 0.005% to 0.01%, and frequency response dc to 10 kHz. Several manufacturers provide VCXOs which meet these general specifications, e.g., Arvin Frequency Devices and Greenray Industries, Inc.

The 10 MHz reference source must also be very stable, with low phase noise. This unit should be an oven-controlled type with a stability on the order of $\pm 1 \times 10^{-9}$ or better. (NOTE: It is possible that this frequency source might be obtained from some other piece of existing ESTL equipment, such as a lab standard, counter, or even the programmable frequency synthesizer discussed in the following paragraph.)

The programmable frequency synthesizer supplies frequencies in the range of 40 to 43 MHz for the purpose of receiver tuning and should have a resolution of at least 0.01 Hz, which translates to better than 2 Hz steps relative to the receiver input frequency. In addition, the sweeping capability should be digitally controlled, and each quantum step must have a continuous phase transition so that phase step transients are not presented to the PLL once it becomes locked but before the frequency sweep is halted.

The Dana Series 7000 Digiphase Synthesizer (in particular, Model 7010-S-179) provides all necessary capability. Digital sweep programming must be externally supplied by either a microprocessor or logic-counter system; thus, it requires specification and design. Phase transitions during frequency steps are continuous. A disadvantage of this model synthesizer is its high cost (approximately \$18K), and to this must be added the digital sweep capability.

Hewlett-Packard's Model 3335A synthesizer (a new market item in late 1977) has a step resolution of 0.001 Hz. It provides automatic full range (settable) single sweep capability over periods of 10 sec or 50 sec from minimum to maximum frequency, which appears to be sufficient.

Unfortunately, stopping and holding control cannot be provided without modification to the synthesizer. Manual sweep at any rate in either the up or down direction may be employed and may be a compromise answer to the sweep problem, especially if the sweep capability is one that will not be regularly used. Phase transitions are continuous for all steps except at the integral 1 MHz points (i.e., at 41 and 42 MHz for the intended application). Thus, although the HP synthesizer has some technical disadvantages, its price of approximately \$8K (compared to the Dana price) could significantly determine whether such disadvantages will be tolerated. The issue is primarily that of the desired

sweep capability and whether it needs to be fully automatic and start/stop controllable at any point for a large number of sweep rates and patterns.

Another possible alternative is to use the HP synthesizer to obtain nominal carrier frequency and sweep the VCXO using an analog waveform. This, however, is not recommended because: (1) if lock is obtained near VCXO band edge, reliable PLL operation may be compromised; (2) holding the VCXO at the correct frequency over a long period of time with an analog voltage and allowing for all types of inevitable drifts could produce significant loop stress; and (3) the analog sweep and control circuits will have higher implementation costs than their digital equivalents. An advantage of sweeping the VCO is that the sweep operation affects only the receiver while, when the programmable frequency synthesizer is swept, the transmitter frequency also changes accordingly.

At this point, the general approach taken to realize the frequency multipliers will be discussed. The direct approach, utilizing step recover diode (SRD) harmonic generators and frequency selective filters, is recommended. Figure 4-6 shows the generic configuration. The input signal at frequency f_0 is amplified to the necessary power level and applied to the SRD through a series resonant filter. Following the SRD, a low-sidelobe (multipole) BPF selects the desired harmonic, and a buffer amplifier raises the power level to the proper level for the next frequency multiplication. A second SRD multiplication takes place, and the output amplifier supplies the MNf_0 frequency at the desired power level.

The highly selective BPFs may be of the LC type for frequencies less than 100 MHz and tubular for frequencies above 100 MHz and where sharp attenuation slope characteristics are needed.

Where the frequency multiplication factor is prime (e.g., X13), only one SRD stage is used. If the multiplication is even (e.g., $X14 = X7 \times X2$), the X2 factor may be more economically realized using a full-wave doubler of the Z-match WD-101 type

The normal or VCO derived $2f_S$ and $2f_L$ frequencies are obtained by mixing the VCXO and programmable frequency synthesizer outputs and selecting the difference frequency with an LC BPF. Similarly, the

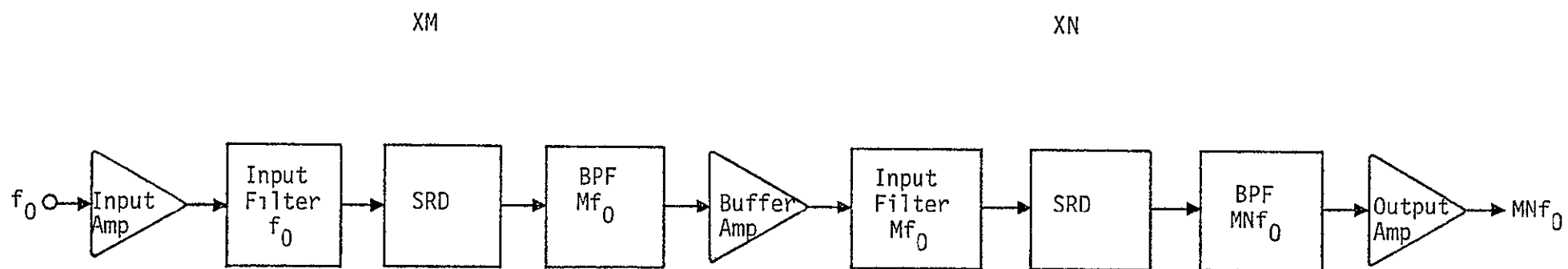


Figure 4-6. Generic Frequency Multiplier Configuration

auxiliary oscillator frequency is obtained from the reference oscillator frequency $\times 6$, mixed with f_{synth} .

The L-band $\times 219/16$ circuit is realized by multiplying $2f_L$ by 13 and by 11/16, mixing, and selecting the sum frequency. Multiplication by 11/16 may be implemented by first dividing $2f_L$ by 16 and then using a $\times 11$ SRD multiplier or a PLL type multiplier. In order to attenuate the mixer difference frequency, the output BPF is specified to be an 8-section tubular with a 3 dB bandwidth of 15 MHz.

Generally, the remainder of the reference frequency synthesis circuits are conventional. Drive amplifiers in the 5-1500 MHz region are Avantek UTC-15 types, while in the 1700-2300 MHz region (first mixer drive), Avantek UTC-23 types are specified.

Lastly, the adjustable phase shifters which allow for the setting of the correct phase of the 10 MHz reference frequency to the AGC, ranging, and command phase detectors are Merrimac Model PS-4-10.

4.1 4 7 AGC and Lock Circuits

The output of the AGC phase detector is low-pass filtered by a single RC section. The time constant, $R_A C_A$, is chosen to meet the AGC loop bandwidth requirements. Two time constants are front panel selectable. AGC voltage is then summed with a variable bias voltage which establishes the nominal AGC loop operating point. The operational amplifier (Burr-Brown type 3500C) output is further low-pass filtered to remove any high frequency spurious signals.

A switch selects between automatic and manual AGC operation. In the manual mode, a front panel potentiometer is capable of setting the VVA over its entire 100 dB operating range.

The AGC voltage is further filtered by an $RC = 10$ sec section and applied to the input of a comparator. An adjustable reference voltage establishes the level above which the receiver indicates lock. A Burr-Brown 4092/03 comparator, with open collector feature, permits any load supply voltage to be used consistent with the output interface desired. (NOTE: The lock indication must be fed to the sweep acquisition circuits as the indicator to disable the sweep action and also to the VCO/Auxiliary Oscillator switch.

4.1.4.8 Command Output Circuits

The command phase detector output is followed by an operational highpass-lowpass filter. The highpass 3 dB frequency of 500 Hz is determined by $R_H C_H$ and the lowpass frequency of 130 kHz by $R_L C_L$. Output voltage gain is R_L/R_H . A Burr-Brown 3500C may be used for this circuit.

4.1.4.9 Ranging Output Circuits

A two-pole, linear-phase, 1.5 MHz 3 dB frequency filter establishes the linear ranging channel lowpass response. The output of this filter is passed to a linear rectifier, followed by an LPF whose output is a measure of the signal-plus-noise level at the linear ranging channel output. Preceding the ranging phase detector is a voltage variable gain amplifier comprised of an RCA CA3002 voltage variable amplifier acting as an attenuator, followed by an Avantek UTC5-146 (+49 dB gain). When the loop is closed, regulation of the linear output signal-plus-noise level to a value established by the bias adjustment is obtained.

The ranging LPF output is also passed through a hard limiter which has a two-level output, preserving only the zero-crossings of the signal-plus-noise. A selector switch is provided to choose between the linear or limited ranging output being applied to the transmitter phase modulator.

4.1.4.10 Phase Modulator and Transmitter Circuits

Phase modulator excitation is obtained by multiplying $2f_S$ by 15 or $2f_L$ by 16. A selector switch (automatically controlled by the receiver lock detector but with manual override) places the transmitter frequency source at the VCO or the auxiliary oscillator. A hybrid splits the $2f$ signal to the X15 and X16 multipliers, whose outputs are selected according to the S-band or L-band transponder configurations.

Figure 4-7 shows the basic mechanization of the phase modulator. A quadrature hybrid has its output ports "shorted" with $f_0 = 30f_S \cong 32f_L$ series resonant filters (LC). The capacitor is a varactor that has been biased into its quasi-linear region of operation. Modulation voltage is applied to the varactors causing, in effect, the short to change its

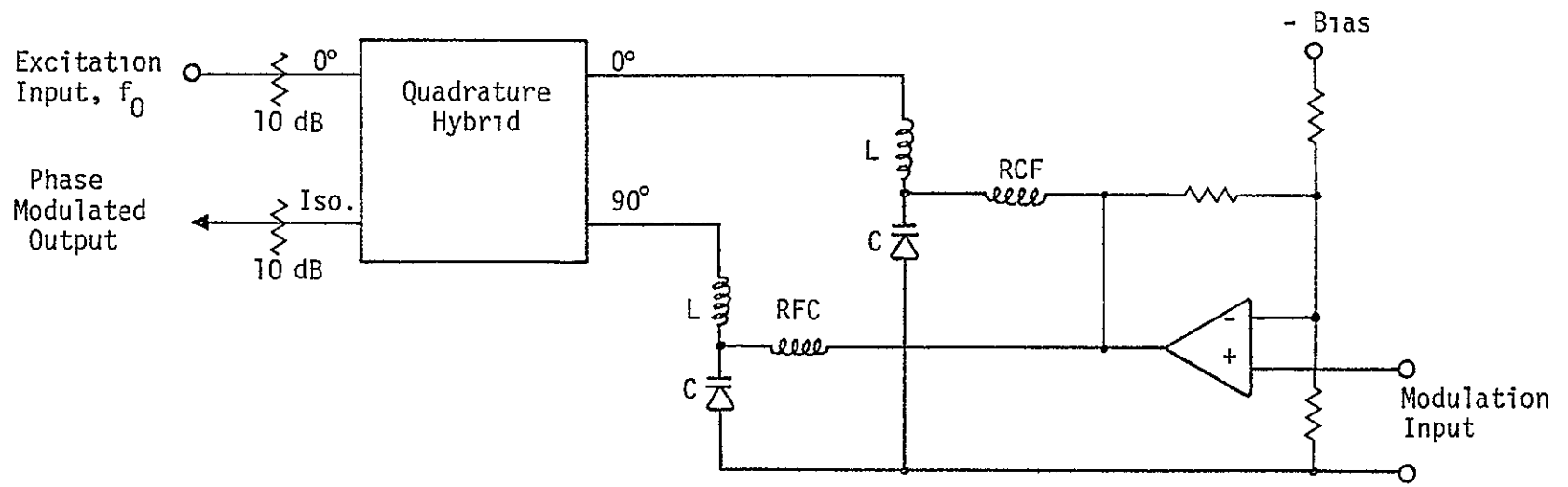


Figure 4-7. Phase Modulator Configuration

resonant point by a small amount. The phase shift arising from the change causes the reflected signals to the isolation port, taken as the phase modulator output, to shift in phase. This action, sometimes referred to as a "sliding short," permits linear phase modulation of the exciting frequency over a limited range ($\pm 18^\circ$ for the subject application).

Driving the phase modulator is an inverting operational amplifier with three simultaneously summed inputs: two telemetry and one ranging. Each input may be switched on or off as desired, and each has an independent modulation index adjusting attenuator. A Burr-Brown 3551L is specified for the summing amplifier. In addition, the telemetry inputs are supplied with line impedance matching differential input amplifiers so that common mode signals from external equipment may be eliminated.

The output of the phase modulator is filtered and input to the X8 multiplier. The BPF is a 4-section tubular type with a 20 MHz 3 dB bandwidth. The output filter of the X8 is also a 4-section tubular with a 3 dB bandwidth of 150 MHz.

A power amplifier with overall gain of 24 dB raises the X8 output to a level of +24 dBm. To realize this capability, an Avantek APT-4036 amplifier (32 dB gain) could be utilized with an 8 dB pad between the X8 output and the amplifier input.

A 30 dB directional coupler (Anaren Model 10616-30, or equivalent) provides a power monitor point for the transmitter low power output. The directional coupler direct port output at +23 dBm (0.2 watts) is taken as the transmitter low power output, used for the cable connecting input to the ESTL RF propagation simulator.

The final power amplifier, which is capable of supplying 2 watts to an antenna feed for air-link operation, may be a solid state or TWTA type. Commercial units can be obtained for this purpose, or a custom design (especially if solid-state) may be accomplished. A 30 dB coupler is used to provide a power monitor point.

4.2 NASA/SGLS Command Detector Unit (CDU)

4.2.1 General Description

In actual flight payload configurations, the CDU is an integral part of the transponder or RF receiver. The CDU demodulates the command signal obtained from the RF receiver and detects the transmitted bits. The detected command data, together with bit timing and CDU lock status, are provided as outputs.

Two distinct types of command signals must be processed by the CDU: (1) NASA types and (2) DOD/SGLS types. The NASA command signal is comprised of NRZ data, biphase modulated onto a 16 kHz subcarrier. Bit rates are selectable in steps of powers of 2, as shown in the following list. The bits are coherent with respect to the subcarrier they modulate.

<u>Bit Rate (bps)</u>	
2000	62.5
1000	31.25
500	15.625
250	7.8125
125	

The SGLS command data is ternary in nature, "1," "0," or "S" symbols are transmitted in an MFSK manner, each having a discrete subcarrier frequency or tone. Data rate clock (at 1/2 the symbol rate) in the form of a triangular signal is amplitude modulated onto the tones. Two symbol rates, 2000 and 1000 symbols per second (sps), are utilized, and the "1," "0," and "S" tones are, respectively, 95 kHz, 76 kHz, and 65 kHz. (See Appendix D for a complete description of the SGLS command waveform.)

4.2.2 Generic Description

Figure 4-8 shows a generic block diagram of the NASA/SGLS CDU. The principal input (i.e., that which comes from the receiver) is through the AGC amplifier. A second input (NRZ input) is provided for testing and calibration purposes. This latter input permits performance evaluation of the NASA bit detector and synchronizer circuits, independent of the subcarrier demodulator.

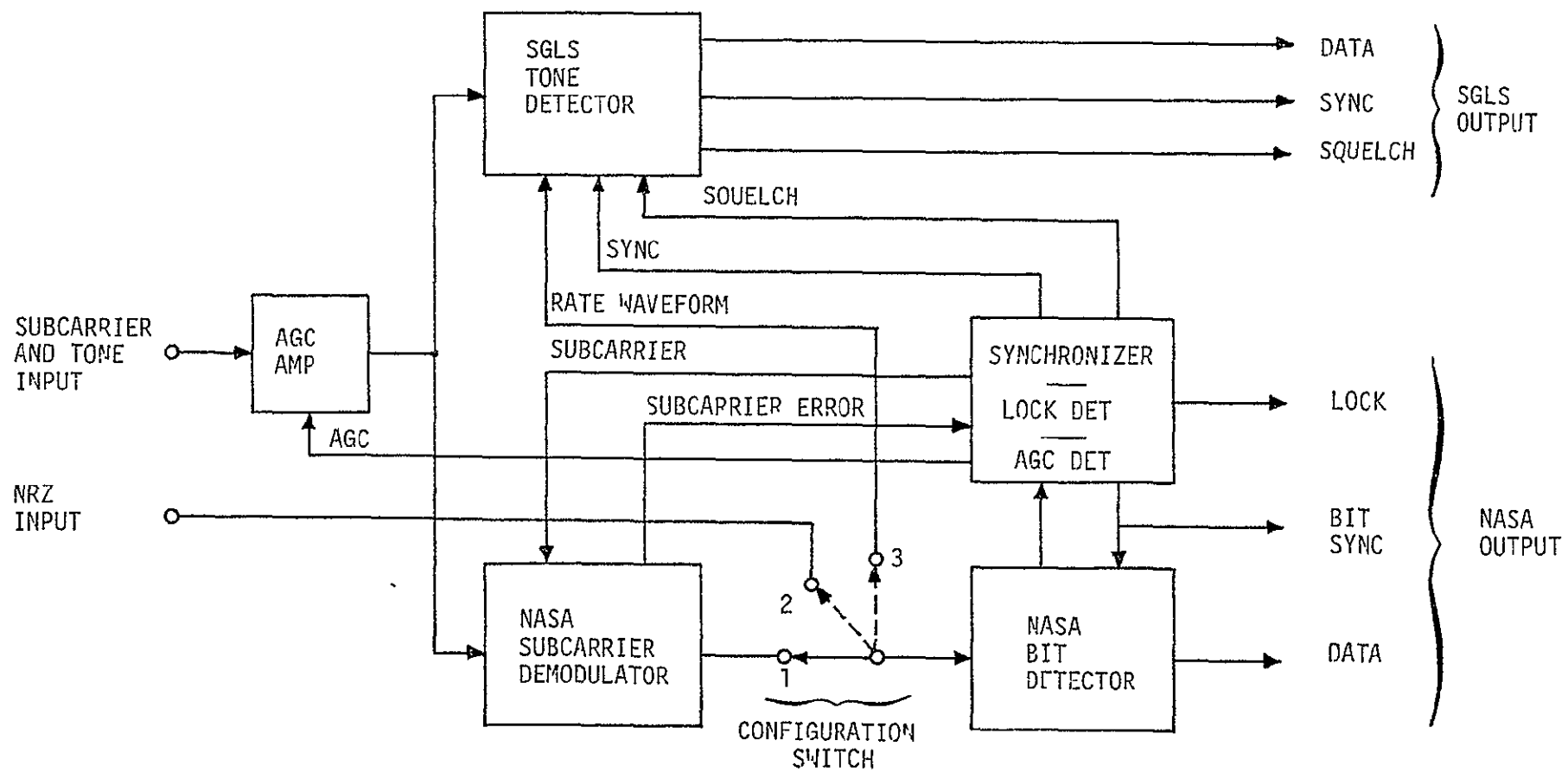


Figure 4-8. NASA/SGLS Command Detector Generic Block Diagram

For proper operation, the input signal amplitude must be maintained within specified limits. Most particularly, fixed reference threshold voltages are employed in the lock/squelch functions, and linear operation must be guaranteed through the analog circuits (e.g., active filters and choppers of Figure 4-12). The AGC amplifier thus functions to regulate the signal level variations out of the receiver,* such that a nearly constant RMS voltage is maintained at the AGC amplifier output. AGC reference values are derived in the detector synchronization circuits.

The SGLS tone detector consists of three frequency selective channels which detect the presence of the command tones. A comparator selects the largest output of the three channels at any given time as representative of which tone or symbol is being received. The detected AM component (rate waveform) is processed by the sync/lock/AGC detector circuits which, in turn, provide noise-free symbol-sync and squelch signals to the tone detector. Sync is used to sample the data output at the optimum time, and the squelch is employed to inhibit data output when the CDU input signal is absent or below threshold.

The sync/lock/AGC detector circuits are common to the distinct NASA and SGLS CDU modes of operation. In a somewhat oversimplified view, the input to the NASA bit detector which functions to pre-process the input signals to the sync/lock/AGC detector, may be switched between (1) the output of the NASA subcarrier demodulator, (2) the NRZ input, or (3) the rate waveform from the SGLS tone detector in order to accomplish the mode changes.

NASA command signals are processed by the subcarrier demodulator to recover the noisy NRZ data bits and subsequently detected using a matched filter. The subcarrier demodulator also produces an estimate of the reference subcarrier frequency/phase-error, which is employed within the sync/lock/AGC circuits to drive the phase error to zero. AGC and lock status are derived from the magnitude of the bit detector

* Although carrier AGC is derived in the transponder receiver and used to regulate the IF circuit gain, it is not sufficient to maintain a constant RMS receiver command output over the full range of received signal level or the extremes of forward link modulation index (especially with ranging on/off).

matched filter values. Bit sync is employed to optimally time the matched filter.

4 2.3 Functional Description

Figure 4-9 is a functional block diagram of the NASA/SGLS CDU. Each of the major functions are described in the following sections.

4 2 3.1 AGC Amplifier

The AGC amplifier establishes a constant, predetermined RMS output signal amplitude to the bandpass filters (BPF) over an input signal dynamic range of 40 dB. Gain control is derived from mean-square values of processed (filtered) components of the input signal, as discussed in Section 4.2 3.5. The response time of the AGC loop is slow compared to any deliberate amplitude variations of the various signals themselves. During acquisition of the CDU (i.e., before subcarrier and/or timing synchronization has been established), the AGC functions, under weak signal conditions, to regulate the RMS value of the CDU input noise voltage. If strong signal conditions prevail, the AGC loop responds to the RMS value of the subcarrier loop (or timing loop for SGLS) beat-frequency. In all cases, the action of the AGC prevents signal amplitude clipping

4 2.3.2 SGLS Data Detector

Three predetection BPFs, each centered on one of the tone frequencies, channelize the input process and provide a sufficiently large SNR (when signal is present) to the detectors. Each filter has the same 3 dB bandwidth (albeit different center frequencies) of four times the symbol rate, or 8 kHz for 2000 sps and 4 kHz for 1000 sps. The BPF characteristics are four-pole Butterworth.

The outputs of the BPFs are input to linear envelope detectors, which produce a filtered version of the BPF output waveform envelope. The post-detection filters are single section lowpass filters (LPF) with a 3 dB frequency equal to the symbol rate. Each of the detector outputs is mutually compared so that only one of the three output data lines can indicate a tone present (i.e., be "true") at any instant of time. If no tones are present (CDU input command signal component is absent), then the squelch disables the output data lines such that all three lines are simultaneously "false "

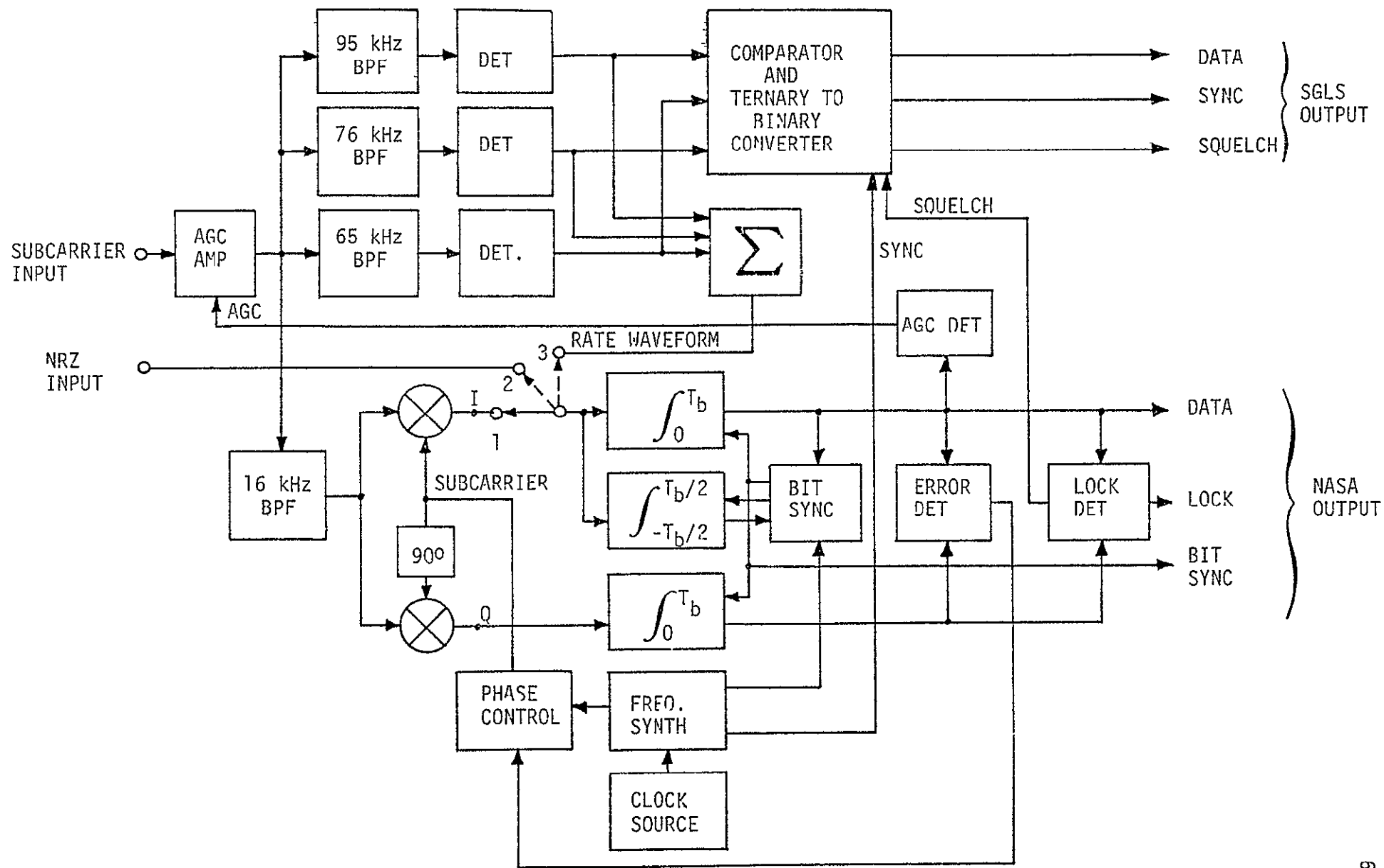


Figure 4-9. NASA/SGLS Command Detector Functional Block Diagram

Provision is made, in conjunction with the sync signal, to convert the three-line ternary output into a single-line binary data stream, where a bit-pair is encoded to represent the three possible received symbols

4.2 3.3 SGLS Sync and Squelch

The three tone detector outputs are summed to produce the SGLS command rate-waveform. For the 1000 sps rate, the waveform is a 500 Hz triangular function, while for the 2000 sps rate, the waveform is a 1000 Hz sinusoid. The sync detector is a sampled-data phase-locked loop which operates on the rate-waveform to generate a phase error signal relative to reference sync clock. In turn, this error is filtered and used to phase correct the sync supplied by the frequency synthesizer to the comparator/converter.

The actual mechanization of the sync detector is a form of the digital-data transition tracking loop (DTTL) (see Section 4.2 3.5 for details). As such, it treats the triangular or sinusoidal rate waveform as an alternating polarity "bit" stream*. Thus, due to the nature of the DTTL operation, a symbol rate (not 1/2 the symbol rate) clock is automatically produced.

The squelch signal is simply the lock indication for the DTTL (see Section 4.2.3 5). When no CDU input command signal component exists, the rate waveform is absent and the DTTL is out-of-lock. However, if an input signal is present, the DTTL rapidly acquires and indicates lock. (Usually a "preamble" of "S" signals is transmitted prior to actual SGLS commanded data, thus providing the necessary time for the DTTL to acquire.)

4.2 3.4 NASA Subcarrier Demodulator and Data Detector

The NASA command signal is pre-demodulation filtered by a 16 kHz BPF. This filter is a high-pass/low-pass type with a lower 3 dB frequency of 8 kHz and an upper 3 dB frequency of 24 kHz. The prime

* Although the "bits" here are not rectangular pulses (but rather triangular or sinusoidal), the digital-data transition tracking loop which integrates over the pulse performs in an essentially waveform insensitive manner

function of this filter is to attenuate noise at the odd multiple frequencies of the 16 kHz subcarrier so that the square-wave reference subcarrier waveform of the demodulator does not fold noise at these harmonic frequencies into the demodulated lowpass bandwidth.

The subcarrier demodulation and tracking loop is of the data-aided loop (DAL) type [6]. The DAL has been selected for the following reasons

1. The NASA Standard CDU, integral to all NASA NE, DS, and TDRSS Standard User Transponders, has a data-aided subcarrier loop.
2. The data-aided loop is somewhat more amenable to digital mechanizations than the Costas loop, especially when multiple data rates are involved.
3. Data rate switching is easily accomplished with the data-aided sampled-process loop, as rate changes involve only the specification of a new internal accumulation index limit. Rate changing with the usual analog Costas loop requires physical switching of the arm filters or their component values. The CDU for the Payload Simulator must operate at eight distinct data rates.
4. It is estimated that the data-aided subcarrier loop, as applied to the Payload Simulator CDU, may be realized for a lower cost than an "equivalent" Costas loop, because it is an existing and proven design for the CDU application. A Costas loop would require design, development, and evaluation of a more fundamental nature; costs would be higher for both engineering and hardware.

Figure 4-10 shows a convenient descriptive model, the loop operating in the following principal manner. The topology of the DAL is very similar to that of the Costas loop; there are, however, major differences. First, the data detector (matched filter) is an integral part of the loop. Secondly, a time delay equal to the bit duration $T_b = 1/R_b$ is employed within the loop.

Subcarrier demodulation is accomplished by multiplying the modulated subcarrier in two phase detectors (multipliers) with reference signals that are in phase-quadrature. When the DAL is in-lock and tracking, the reference $r_1(t)$ is in-phase with the subcarrier, while the reference $r_2(t)$ is at a phase of 90 degrees with respect to that of the subcarrier. The signal $e_1(t)$ represents the demodulated data

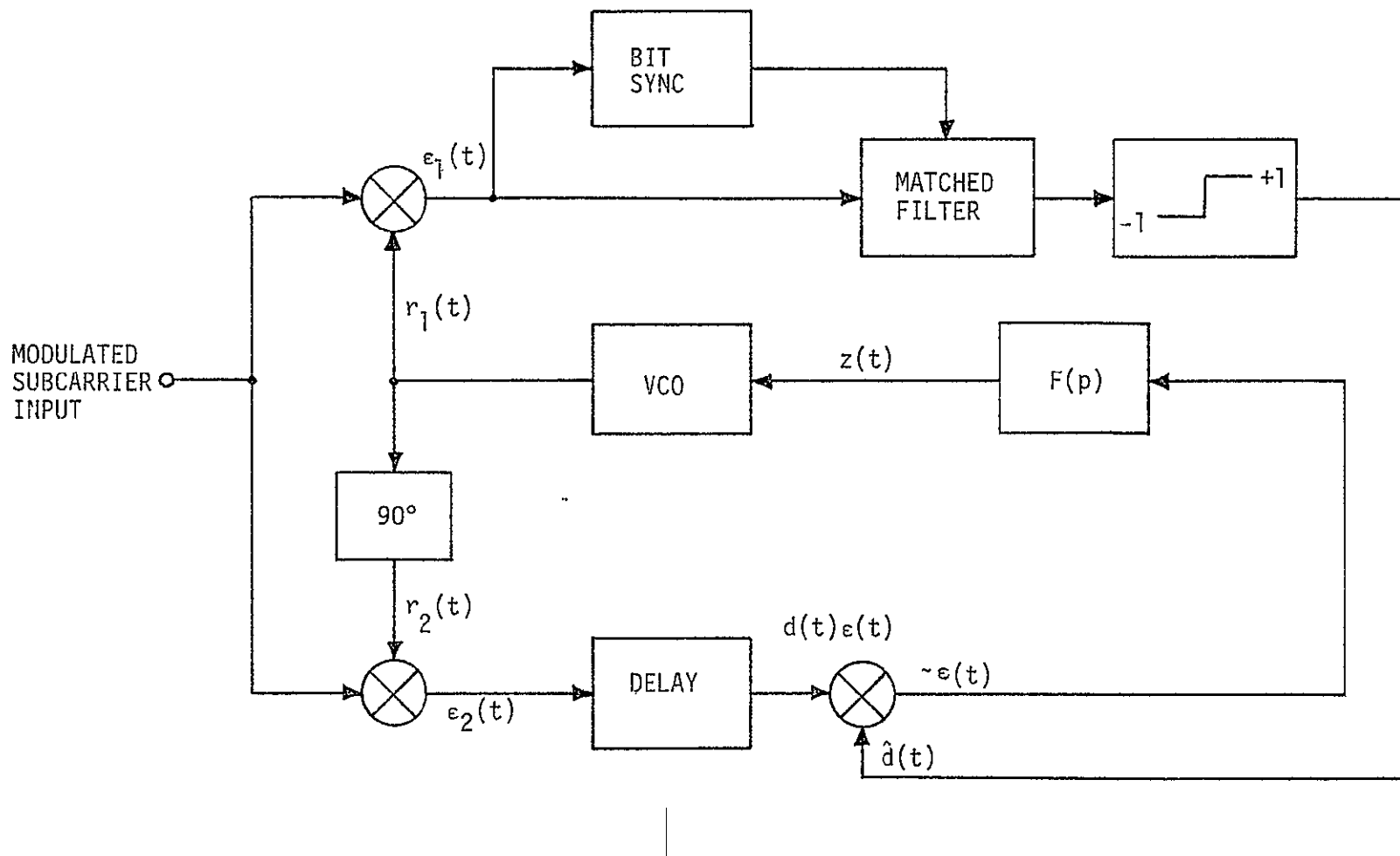


Figure 4-10. Data-Aided Loop Model

bits and $\epsilon_2(t)$ is proportional to the subcarrier/reference phase error.

The basic idea of a data-aided loop centers around using the power in the composite received signal (data-modulated subcarrier) sidebands to maximize the signal-to-noise ratio in the bandwidth of the subcarrier tracking loop. The method by which this is accomplished employs the principle of decision-directed feedback.

Demodulated data bits are matched filtered (this is an integrate-and-dump operation) and hard decisions are made as to whether a "1" or a "0" has been received, the received bit stream being designated at $\hat{d}(t)$. The error signal $\epsilon_2(t)$, which is modulated by the data stream, is time delayed by the period of one data bit so that its data stream, $d(t)$ is time coincident with that of $\hat{d}(t)$. Multiplication of the two signals (Figure 4-10) produces $\hat{d}(t)d(t)\epsilon(t)$. Now, since $\hat{d}(t)$ is a highly credible estimate of $d(t)$ (the bit error probability is by definition less than 1×10^{-5}), the product $\hat{d}(t)d(t)$ is essentially unity. Thus, "anti-modulation" takes place, with the result that

$$\hat{d}(t)d(t)\epsilon(t) \approx \epsilon(t).$$

$\epsilon(t)$, a pure error signal, is then filtered and applied to the VCO so that the phase error is driven to zero.

Returning now to Figure 4-9, the data-aided subcarrier loop is implemented in the following general manner. The outputs of the two quadrature phase detectors (I and Q) are both integrated over the bit period, T_b . Data bit estimates are the sign of the I-channel integrator. The Q channel integrator serves to integrate the error-proportional signal, thereby acknowledging the needed delay. It should be noted that the filtering effects of this integration are of no consequence to the loop operation, as the DAL tracking bandwidth is much less than the inverse of the bit period. The data estimate serves to multiply the algebraic sign of the Q-channel integrator (ERROR DET), thus producing the modulation-free error signal. Note at this point that the operation passes from a time-continuous to a time-discrete process, as the error signal is produced only at the end of the integrator bit periods when the signal-to-noise ratios are maximum. Actually, as will be explained in Section 4.2.4, the mechanization of the entire integration process is carried out in a sampled data fashion.

The clock source provides the master frequency to the frequency synthesizer which, in turn, produces the necessary timing signals for the CDU. Subcarrier reference frequency is phase-controlled by the DAL error signal in order to effect proper lock of the subcarrier loop.

5.2.3.5 Sync, Lock, and AGC Detectors

Figure 4-11 shows the basic configuration of the digital data transition tracking loop (DTTL).

The I-channel data signal is integrated on the bit period as discussed in Section 4.2.3.4, and decisions are made resulting in the bit stream, d_1 . This bit stream is clocked into a one-bit memory so that successive bit pairs are simultaneously available. A transition detector, $T_1 = \hat{d}_{1-1} - \hat{d}_1$, is formed to determine whether successive bits change polarity and in which direction.

A second integrator, also operating on the I-channel data signal, has its integration period over one bit time offset from that of the data decision integrator by 1/2 bit period. This integrator is referred to as the mid-phase integrator. The output of the mid-phase integrator, when there is bit timing error and given that a data transition takes place during its integrating period, is proportional to the bit timing error. This result is "held" until the transition detector determines whether, in fact, a transition has occurred. A product is then formed between the error signal and the transition detector output to produce the term, $T_1 \epsilon_{b1}$. This term is always sense-wise proportional to the error, irrespective of the direction (1 to -1, or -1 to 1) of the transition. If no transition takes place, the term is 0 (as it should be, because the mid-phase integrator output will not be proportional to error unless a transition is present).

K successive nonzero $T_1 \epsilon_{b1}$ values are summed (filtered) before a decision is made to adjust the bit clock phase in the direction which reduces the bit timing error. Thus, bit sync is acquired and maintained in the presence of slow bit clock drift.

Referring again to Figure 4-9, the DTTL synchronizer is comprised of the two integrators with inputs from the I-channel, plus the box labeled BIT SYNC. As noted in Section 4.2.3.3, it also serves to synchronize to the "rate-waveform" produced when the CDU is in the SGLS mode.

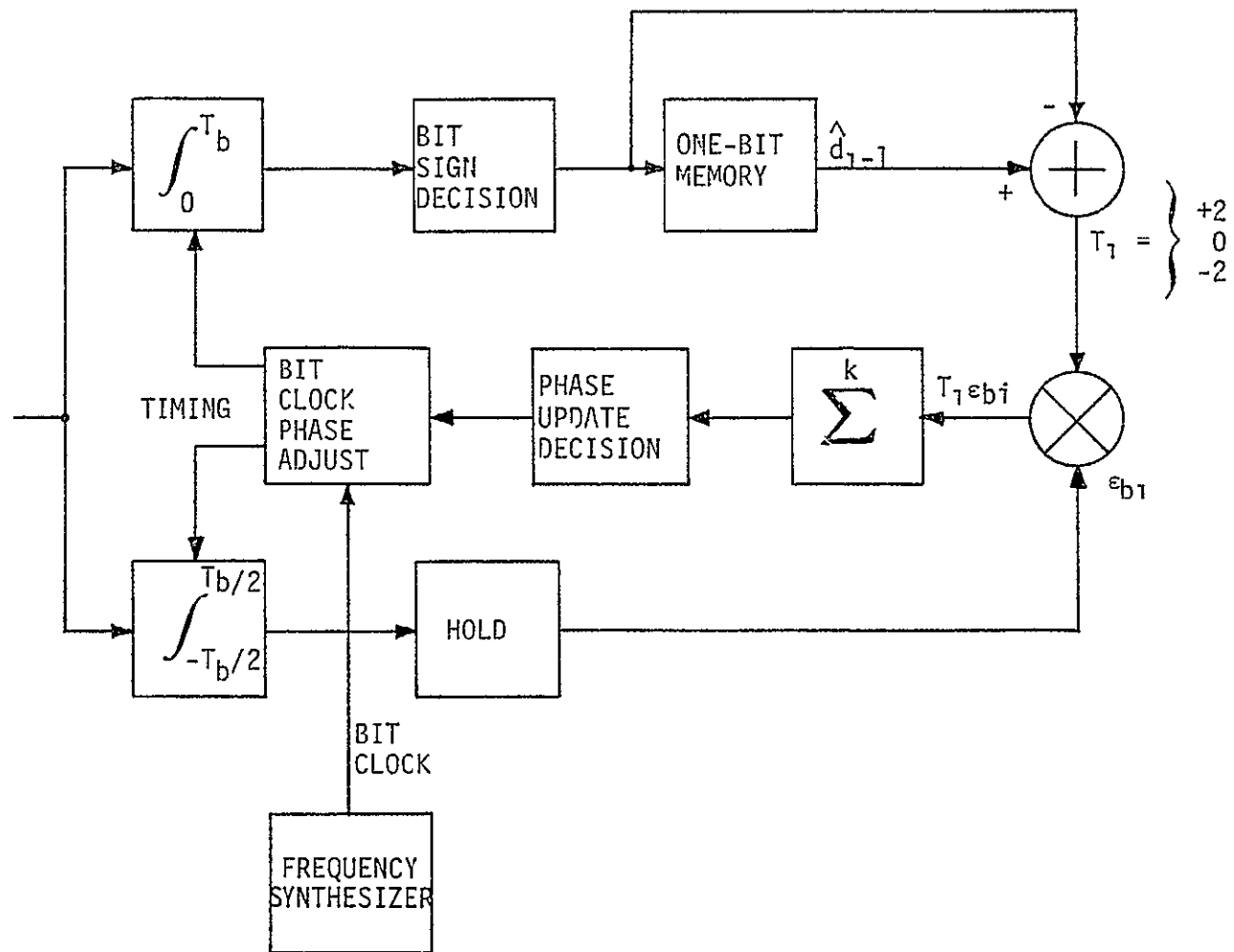


Figure 4-11. DTTL Sync Detector

The lock signal is derived by subtracting the magnitude of the Q-channel integrator output from the magnitude of the I-channel integrator. These differences are accumulated over a fixed number of bit periods and then compared to a threshold voltage. In-lock is declared when a number of successive lock signal values fall above the threshold. Out-of-lock is declared if two or more successive values are below the threshold.

AGC control is obtained simply by using the magnitude of the I-channel integrator as a measure of signal-plus-noise power. When a signal is absent, the detector gain is set at its maximum value (i.e., the AGC amplifier has its maximum gain), commensurate with no noise peak clipping in any analog circuits. With a signal present, the measure of signal-plus-noise power must, of necessity, increase. The proper signal power will not be determined until the bit-sync loop (and subcarrier loop, if applicable) becomes locked. As such, some signal clipping could take place in the analog circuits but with no significant ill effects on acquisition performance. When the true value of the signal power is obtained, the AGC regulates so as to maintain the RMS value of signal-plus-noise to a predetermined level. A sufficiently long time constant is used for the AGC loop to preclude regulation to anything but gross CDU input changes.

4.2.4 Detailed CDU Implementation

The following sections present a detailed discussion of how the CDU should be implemented in order to meet the requirements of the Payload Simulator at a reasonable cost.

It should be noted that exact replications of the NASA and SGLS CDUs are not advocated. The general approach taken is that of realizing each of the needed functions through maximum use of commercially available components and assemblies. Where custom design is necessary, proven approaches, such as the extensive use of operational amplifier based analog circuit configurations, are recommended.

Figure 4-12 shows the detailed CDU block diagram, to which reference will be made in the following sections.

4.2.4.1 AGC Amplifier Circuits

The subcarrier input signal is isolated from the voltage variable gain circuits by means of a differential amplifier configuration. The input signal cable shield (or wire-pair common lead) is floated relative to the CDU chassis so that the differential amplifier may remove all common mode noise components. Input resistance, R_{in} , is selected to match the input cable impedance. The differential amplifier gain is unity.

In order to accommodate a dynamic range of 40 dB, a balanced-diode voltage variable attenuator (VVA) circuit is recommended. Commercially, this may be realized by a monolithic chip such as the National LM170. A Motorola discrete-component design [7] for the NASA Standard CDU could also be adopted. The gain of the amplifier following the VVA is 40 dB while the overall VVA/amplifier combination should provide a linear AGC voltage-to-gain range of +15 dB to -25 dB.

4.2.4.2 SGLS Active Bandpass Filters

Many versions of the SGLS command detector (signal conditioners) exist with differing performance characteristics. In many mechanizations, the tone filters are double-tuned, critically coupled RLC networks. Because of the requirement to have the simulator SGLS detector operate at both 1 and 2 ksps data rates, active filters have been selected as the most judicious method of implementation. The needed filter characteristics are shown in Table 4-2. The 4-pole filter characteristic may be realized through the cascade of two operational filters of the configuration shown in Figure 4-12. Component selection procedures are available in many references or application notes (see, for example, [8]). Bandwidth and gain switching are accomplished by changing the values of the three resistors in each operational filter section.

4.2.4.3 SGLS Detectors and Rate Filters

An operational, linear half-wave rectifier is to be employed as the BPF output envelope demodulator. Smoothing (symbol filtering) is accomplished via an RC lowpass filter (LPF). A voltage follower between the rectifier and LPF prevents loading of the rectifier circuit and provides a very low impedance source for the LPF. Two LPF time constants, RC and $RC/2$, are provided for the 1000 and 2000 sps data rates, respectively.

Table 4-2. SGLS BPF Characteristics

Symbol Rate (sps)	Tone Frequency (kHz)	Filter 3 dB BW (kHz)	Number of Poles	Center Frequency Gain (dB)
1000	65	4	4	24
	76	4	4	24
	95	4	4	24
2000	65	8	4	18
	76	8	4	18
	95	8	4	18

The outputs of the three envelope demodulators (taken from the voltage follower outputs) are operationally summed with a voltage gain of 4 and lowpass filtered by a single-section RC filter with 3 dB frequency of 4 kHz. AC coupling is used on the summer input ($R_S C_S = 10$ sec) to eliminate the direct voltage component due to the mean tone level, leaving only the 1/2 symbol rate periodic clock modulation (i.e., the rate waveform) at the output of the summer.

4.2.4.4 SGLS Comparators, Decision, and Converter Circuits

The comparators are differential input types with a TTL-compatible (0-5V) output. National LM 111 or equivalent types will serve for this function.

Recovery of the ternary information is accomplished by combining the comparator outputs according to the logic equations of Table 4-3. NOR logic for this operation is shown in Figure 4-12.

Table 4-3. SGLS Data Recovery Logic

"1" True	=	$X \bar{Z} L$	=	$\overline{\bar{X} + Z + \bar{L}}$
"0" True	=	$Y \bar{X} L$	=	$\overline{\bar{Y} + X + \bar{L}}$
"S" True	=	$Z \bar{Y} L$	=	$\overline{\bar{Z} + Y + \bar{L}}$

Normal output from the SGLS CDU consists of the three possible information states, each on its own line. In order to process the command information in the ESTL Univac computer, it is necessary to encode the ternary output into a single binary data stream. This is accomplished in the converter, the encoded data format is tabulated in Table 4-4. (The ternary state 000 is called the squelch state, where all three lines are false because no tone signals are present or the SNR is sufficiently low that an error probability of 10^{-5} or less cannot be guaranteed.) The structure of the binary serial stream places Bit B ahead of Bit A in time (or Bit B occupies the odd bit positions and A the even). For the ternary symbol rate of 1000 sps, the serial binary data stream is at a rate of 2000 bps, while 2000 sps results in a 4000 bps serial stream.

Table 4-4. Ternary-to-Binary Conversion

"1" Line	"0" Line	"S" Line	Binary Bit A	Binary Bit B
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
1	0	0	1	1

Symbol clock and the squelch state are provided for external use, with the squelch being displayed as a light on the simulator front control panel.

An extensive output signal switching configuration (not shown in Figure 4-12) permits the ternary signals to be processed by external equipment such as decryptors, etc. (See the Appendix A specification, Section 3.2.2.8).

4.2.4.5 NASA I and Q Subcarrier Demodulators

The subcarrier demodulator input filter (F_4 on Figure 4-12) is a cascaded operational high-pass/low-pass pair as shown in Figure 4-13.

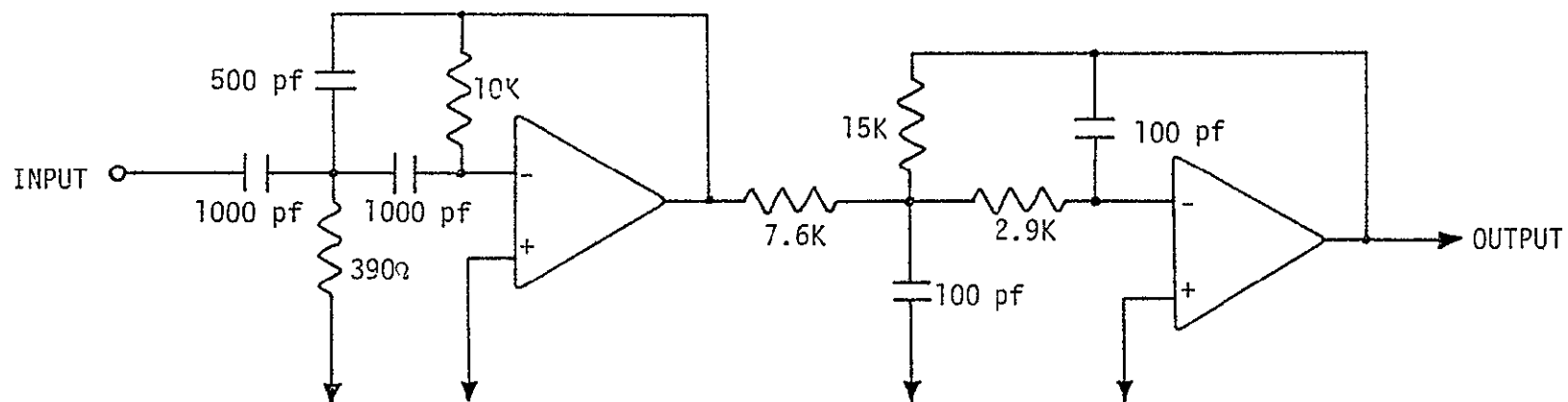


Figure 4-13. 16 kHz Subcarrier Demodulator Input Filter

Each section has two poles with a passband voltage gain of 2; typical component values are shown.

A number of approaches may be taken to realize the chopper phase detectors. A monolithic 4-quadrant multiplier might be used (e.g., Signetics MC 1596); however, bipolar reference signals are required (necessitating differential level converters operating from the subcarrier waveform TTL logic circuits), output voltage followers would be needed, and balance and voltage offsets could be a problem. Balanced diode ring-bridge transformer coupled mixers could be employed, but the lower sub-carrier frequency of 16 kHz dictates that a custom design would be needed, as few commercially available units will work at this frequency. The best approach is to use a MOS analog switch configuration (e.g., National LH 0014) in conjunction with an operational phase splitter (see [9] for circuit information). Such a configuration provides excellent input and reference signal isolation, linear transfer characteristics, and good balance. Logic level drive circuits preclude the need for a bipolar reference waveform.

The LPFs following the subcarrier demodulators have a six-pole characteristic and a 3-dB frequency of 8 kHz. The sharp roll-off is needed to attenuate the 32 kHz harmonic of the subcarrier created by the demodulation process and to permit the use of a 16 kHz sampling frequency without significant aliasing error. This filter may be realized by the cascade of two 3-pole operational amplifier-based lowpass sections.

The NRZ input to the CDU is a differential amplifier identical to that employed for the normal subcarrier input. A switch permits the NRZ signal to be input to the I-channel 6-pole LPF in place of the chopper demodulator output. (Note that an AGC capability is not provided for the NRZ input which is used only for calibration purposes. Thus, care must be exercised so that the signal-plus-noise voltage at the ADC input point is properly scaled.)

4.2.4.6 Multiplexer, ADC, and DAC

Sampling of the I and Q channels is accomplished at the rate of 16 kHz for each channel. In order that only one ADC be required, the input to the ADC is multiplexed (switched) between the I and Q signals every 31.25 μ sec, and the ADC operates at a sampling rate of 32 kHz.

The same type of MOS switch that is used for the chopper subcarrier demodulators (e.g., National LH 0014) can be used to implement the multiplexer.

A switch allows the ADC input to receive a signal from the multiplexer in the NASA mode or from the envelope summer/filter output (rate waveform) in the SGLS mode. The ADC is a successive approximation 8-bit* (7-bit magnitude plus sign) type, with an input range of ± 5 volts. Conversion rate is a fixed 32 kHz for all modes and data rates.

The DAC is used to convert the AGC magnitude digital value (see 4.2.4.7) into a discrete continuous voltage. Ten-bit accuracy is employed, with a voltage range of 0 to 2.5 volts.

The AGC loop is closed through a lowpass smoothing filter, and the AGC voltage is summed in an operational amplifier with NASA and SGLS selectable reference voltages. Amplifier output is applied to the VVA.

4.2.4.7 Sampled Data Algorithms

The following subsections outline the logic and computational algorithms that produce the timing clocks, integration/detection, data transition detector and bit sync phase control, subcarrier phase error and correction, and lock detection. Implementation is recommended using TTL integrated circuits (e.g., Series 74), although portions are amenable to microprocessors. Tradeoffs will be discussed in Subsection 4.2.4.7.5.

4.2.4.7.1 Clock Frequency Synthesis, and Phase Control

The crystal-controlled master clock source operates at a frequency of 512 times the subcarrier frequency of 16 kHz, or $f_{CL} = 8192$ MHz. The frequency synthesizer is therefore comprised of a number of divider circuits, producing clocks and indexes at various frequencies and phases to operate the serial arithmetic functions (principally the accumulators) and generate the subcarrier and bit-rate waveforms. Provision is made for adjusting the phase of the NASA bit-sync and SGLS symbol-sync clocks that are transmitted to the simulator output interface.

Phase control of the subcarrier and sync waveforms for the purpose

* Eight bits are used in the NASA Standard CDU and have been determined to be a good design value for DAL operation (see [6]).

of subcarrier and sync loop tracking is accomplished by adding or deleting divider trigger transitions at the appropriate frequency level in the frequency synthesizer. Control for these functions is supplied by the bump-accumulators (loop filters) explained in Subsection 4.2.4.7.4.

4.2.4.7.2 Accumulators (Integrators)

Integration of sampled-data signals is accomplished simply by adding or accumulating sample values. To realize a matched filter, the accumulator begins in the reset state and sums a predetermined number of samples, at which point its contents become the matched filter value. The accumulator is then reset and the operation is repeated.

The two in-phase and one mid-phase accumulators shown in Figure 4-12 must each sum eight ADC samples at $R_b = 2000$ bps and $256 \times 8 = 2048$ samples at $R_b = 7.8125$ bps. Thus, these accumulators must be 19 bits in size.

It is noted here that data rate changes (by a factor of a power of 2) are accomplished simply by changing the accumulator indexes. This then precludes the need to switch the bandwidth of the 6-pole sampling lowpass filters as the data rate is changed.

The other accumulators shown in Figure 4-12 have the following sizes.

<u>Accumulator Identification</u>	<u>Index</u>	<u>Size (bits)</u>
Magnitude	$N = 8$	13*
Subcarrier Bump	$J = 16$	23
Bit-Sync Bump	$K = 4$	21
AGC	$L = 32$	18**

4.2.4.7.3 Complementation (Multiply)

The detected data bit multiplies the output of the I-channel mid-phase accumulator and the Q-channel in-phase accumulator to produce, respectively, the bit-sync and subcarrier phase error signals. These operations are straightforwardly accomplished by means of the one's-complement of the holding register output.

* The inputs to these accumulators are scaled as a function of data rate to be the largest 10 bits from the in-phase accumulators.

** Only the 10 most significant bits are output to the AGC DAC.

4.2.4.7.4 Bump Control

The phase of the bit-sync clock and subcarrier frequency is controlled in the frequency synthesizer as indicated in 4.2.4.7.1. Because there is no doppler or significant frequency drift to track, only first-order phase correction is needed. This is accomplished by bumping (shifting) the phase of the bit sync clock $\pm 1/8$ bit, depending upon the sign of the bit-sync bump accumulator and, likewise, the phase of the subcarrier $\pm 1/32$ of a cycle, akin to the sign of the subcarrier bump accumulator.

For the in-phase and mid-phase accumulators, the bit-sync bump simply changes the point at which accumulation begins by ± 1 ADC sample. (Note that the bit-sync bumps will come at irregular times because the bit-sync bump accumulator is increased only if a data transition has occurred.)

4.2.4.7.5 Hardware Logic Versus Microprocessors

The entire sampled-data algorithm may be implemented with Series 74 TTL. Exclusive of the ADC, DAC, and crystal clock source, it is estimated that no more than 140 14-pin and 16-pin dual-in-line ICs would be required.

Much of the sampled data algorithm is amenable to the use of a microprocessor. Excluding the frequency/clock synthesis logic and perhaps the in-phase and mid-phase accumulators, microprocessor subroutines can handle the data transition detector, data and subcarrier bump generation, magnitude/lock and AGC accumulations, and lock detector threshold comparisons. In addition, the microprocessor could compute SNR and other measurement/status indicators as discussed in Appendix C of this report.

For a single simulator implementation, the use of a microprocessor will not save on cost over the hardware logic approach, but does add flexibility and additional capability * For pricing purposes, hardware logic has been assumed

* The design of the hardware logic is straightforward. Use of a microprocessor will likely involve the need to design interface buffers and decoders, as well as the time needed to generate and check out the operating program. Thus, the same and perhaps more engineering hours would be required for the microprocessor versus the hardware designs.

4.3 Telemetry Modulators

4.3.1 General Description

The telemetry modulators consist of subcarrier waveform generators capable of being biphase modulated by digital data or frequency modulated by digital or analog waveforms. The outputs of the modulators are input to the transmitter phase modulator where they become the sidebands of the S-band signal.

4.3.2 Generic Description

Figure 4-14 shows the generic block diagram of the telemetry modulators. Two types of modulators are employed: (1) a phase-shift-keyed (PSK) modulator and (2) a frequency modulator (FM).

For the PSK modulator, a stable subcarrier sinusoidal waveform at frequency f_1 (1.024 MHz or 1.7 MHz) is generated. The modulating data stream $d(t)$ is a random sequence of bits represented by a two-level waveform with amplitude of +1 or -1. The biphase modulator acts to output the subcarrier waveform when $d(t)$ is +1, and minus the subcarrier waveform (i.e., a 180° phase reversal) when $d(t)$ is -1. Mathematically, the PSK modulator output is of the form:

$$S_{\text{PSK}}(t) = d(t) \cos(2\pi f_1 t) = \sin\left[2\pi f_1 t + \frac{\pi}{2} d(t)\right].$$

The frequency modulator acts to linearly deviate the nominal subcarrier frequency f_2 (1.7 MHz) in proportion to the modulating waveform $m(t)$. Instantaneous frequency is therefore given as:

$$f_I = f_2 + km(t),$$

where k is a sensitivity factor. A mathematical representation of the FM output is:

$$S_{\text{FM}}(t) = \cos\left[2\pi f_2 t + 2\pi k \int_0^t m(\alpha) d\alpha\right].$$

4.3.3 Functional Description

Functional block diagrams of the telemetry modulators are shown in Figure 4-15.

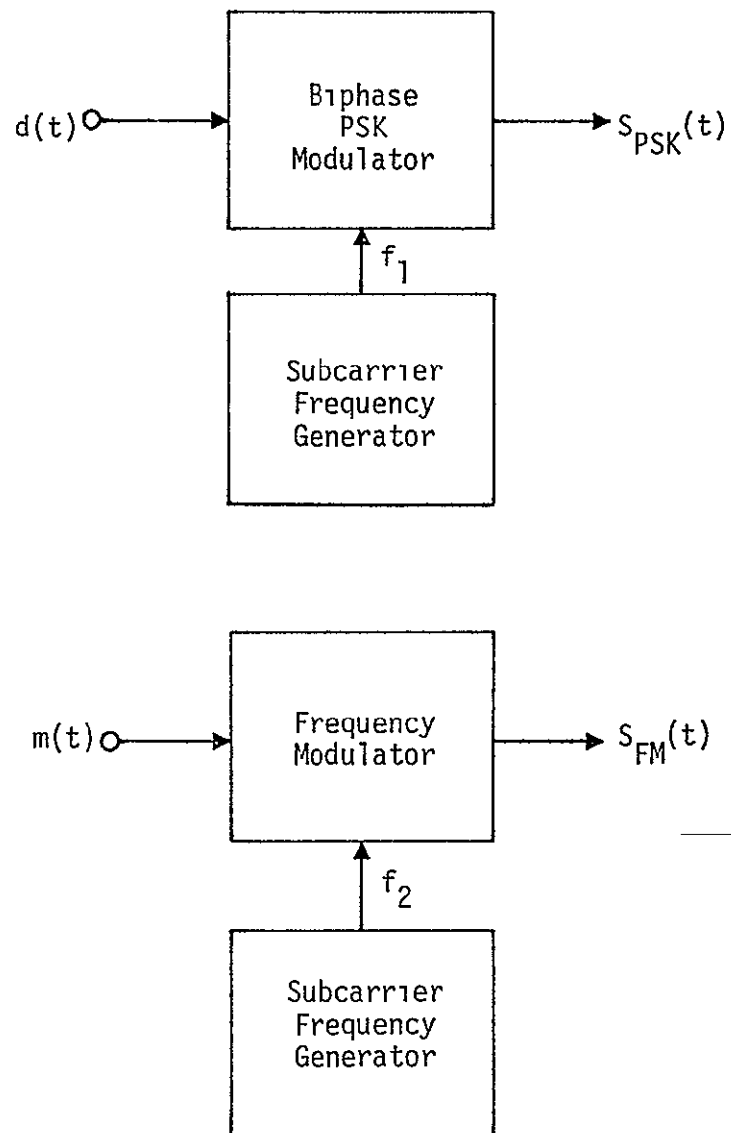


Figure 4-14 Generic Telemetry Modulators

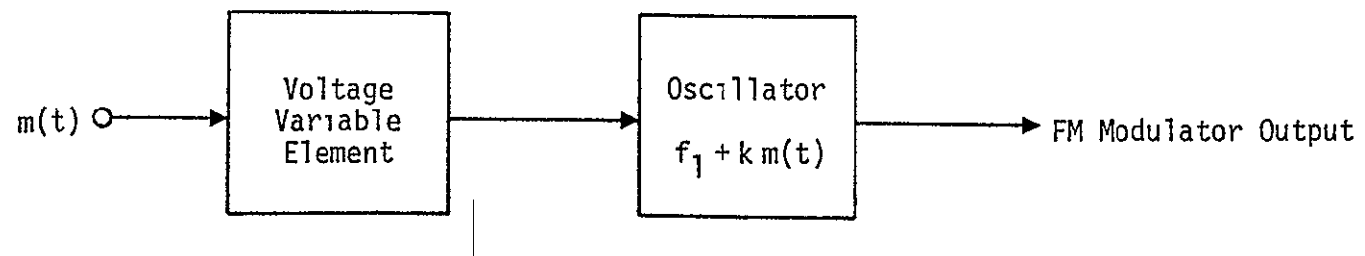
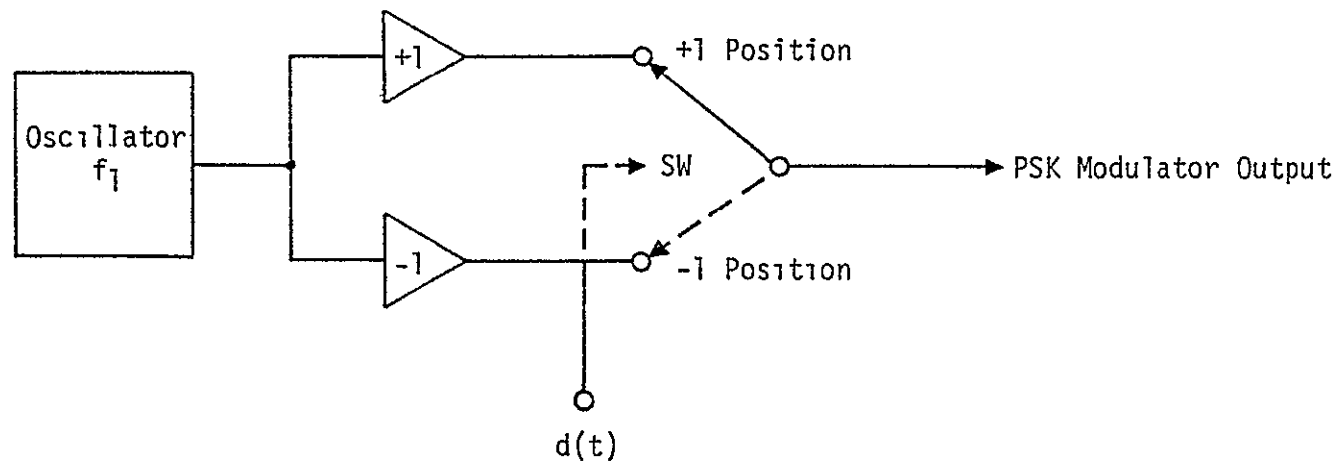


Figure 4-15. Functional Telemetry Modulators

The PSK modulator consists of an oscillator source which produces the frequency f_1 . Two amplifiers (buffers), one with a gain of +1 and the other with a gain of -1, provide antipodal or phase-split versions of the oscillator's signal to the phase switch, SW. The phase switch is instantaneously in either the +1 or -1 position, depending upon the polarity of the $d(t)$. Thus, at the output, effective modulation is accomplished.

Frequency modulation is obtained by a direct process. The frequency of the oscillator is determined by either a timing or resonant circuit which contains an element whose value can be altered by the modulating voltage, thus causing a change in the timing or resonant conditions. If a multivibrator oscillator is employed, the element is effectively a voltage variable current source which controls the rate of charge of the multivibrator capacitors. When an LC type oscillator is used, a voltage variable capacitance (varactor) is instrumental in changing the resonant frequency. Both of these approaches are discussed in detail in Section 4.3.4.

General specifications for the modulators are listed in Table 4-5.

Table 4-5 Telemetry Modulator Specifications

Parameter	PSK Modulator	Frequency Modulator
Subcarrier Frequencies	1.024 and 1.7 MHz	1.7 MHz
Modulation Response	0 bps to 256 kbps	100 Hz to 200 kHz
Peak Deviation	$\pm \pi/2$ radians	± 160 kHz
Output Bandwidth	400 kHz	500 kHz

4.3.4 Detailed Implementations

4.3.4.1 PSK Modulator

Biphase modulator implementation at a subcarrier frequency on the order of 1 MHz is somewhat difficult. Two general approaches have been

investigated (1) use of J-FET or MOS-FET chopper switches in conjunction with an operational phase splitter and combiner and (2) transformer/diode double balanced mixers

The FET chopper approach suffers from switching rate and transfer frequency limitations, plus the need for drive level (switching) translators that have "odd" supply voltage requirements. Many FET switches exhibit transfer roll-off characteristics at 1 MHz and above requiring that, when they are used in chopper applications, they be selectively "matched" so as to maintain good chopper balance. A second problem is that the transient switching times and delays, which are different between on-to-off and off-to-on states, will cause amplitude irregularities on the output waveform of the chopper. When MOS-FET switches are employed, there are additionally large switching transients ("spikes") that occur on the output, requiring minimization by means of output filters. Perhaps most important are the special supply voltage requirements of the drive translators. Most FET switches when used for chopper service require an "on" drive voltage of +10V and an "off" drive voltage of -20V. Normally, the digital and analog circuits that comprise the bulk of the telemetry modulator (and transponder and CDU) need power supply voltages of +5V (for TTL logic) and $\pm 15V$ (for amplifiers, etc.). Although the +10V could be obtained by using a regulator off the +15V supply, there is no equivalent means of deriving the -20V. Thus, a separate power supply is required.

Examining next the limitations of double-balanced mixers, the most obvious problem is that few commercially produced mixers are designed to work at 1 MHz. Even when 1 MHz is the manufacturer's lower specified limit, conversion loss will be high and balance a likely problem. Additionally, good performance is predicated on proper impedance (50-ohm) matching of all ports, requiring judicious design of the drive and output circuits.

After detailed study of the two basic approaches to biphase modulator design, it was decided to recommend in favor of the balanced mixer approach. The prime motivation for this choice stems from the fact that Merrimac Industries produces a mixer whose lower frequency limit is specified to be 20 kHz and, from the manufacturer's typical characteristic information, it has been judged that very good biphase modulator

performance will be obtained at 1 MHz.

Figure 4-16 shows the detailed diagram for the biphase telemetry modulator. The 1.024 MHz or 1.7 MHz source is a crystal oscillator (e.g., Ferwalt Model X045 or similar unit). The output impedance Z_0 is matched by the input resistor (R_0) to the operational amplifier (Burr-Brown 3341/15C). Amplifier gain is selected so that the amplifier output delivers a +7 dBm power level to the L-port input of the double balanced mixer.

A Merrimac Model DMS-2-50 mixer is specified. Output is taken from the R-port, which is terminated by the 50-ohm input resistor to the output operational amplifier (Burr-Brown 3341/15C). The gain of the output amplifier is set to provide a modulator output voltage which will drive the transmitter phase modulator to beyond its maximum specified deviation when the input attenuator is minimum (see Section 4.1.4.9 and Figure 4-3).

Modulation drive to the mixer is ± 40 ma, supplied from a current driving amplifier (Burr-Brown 3553AM) through a matching network which loads the X-port with 50 ohms. Voltage drive to the current amplifier is supplied by a differential amplifier configuration (Burr-Brown 3550J), which converts the data TTL logic voltage levels (0V, 5V) to ± 9 V.

Provision is made for two data inputs selectable by logic control levels. The input configuration is a dual differential line receiver of the National DS55107 type.

4.3.4 2 Frequency Modulator

FM requirements for the various SGLS configurations appear to be somewhat diverse. Disregarding voice,* the PAM/FM and FM/FM requirements dictate deviation sensitivities of ± 30 kHz and ± 160 kHz, and input modulation bandwidths of 20, 50, 100, and 200 kHz.

Flight implementations of the 1.7 MHz frequency modulators usually make use of the voltage-frequency-controlled astable multivibrator circuit, because it is simple (and low cost) to implement and has reasonably linear large deviation characteristics. The problems with this approach are that (1) stability is poor and center frequency drift can

*Voice is not used for the applicable payload simulated missions.

0-2

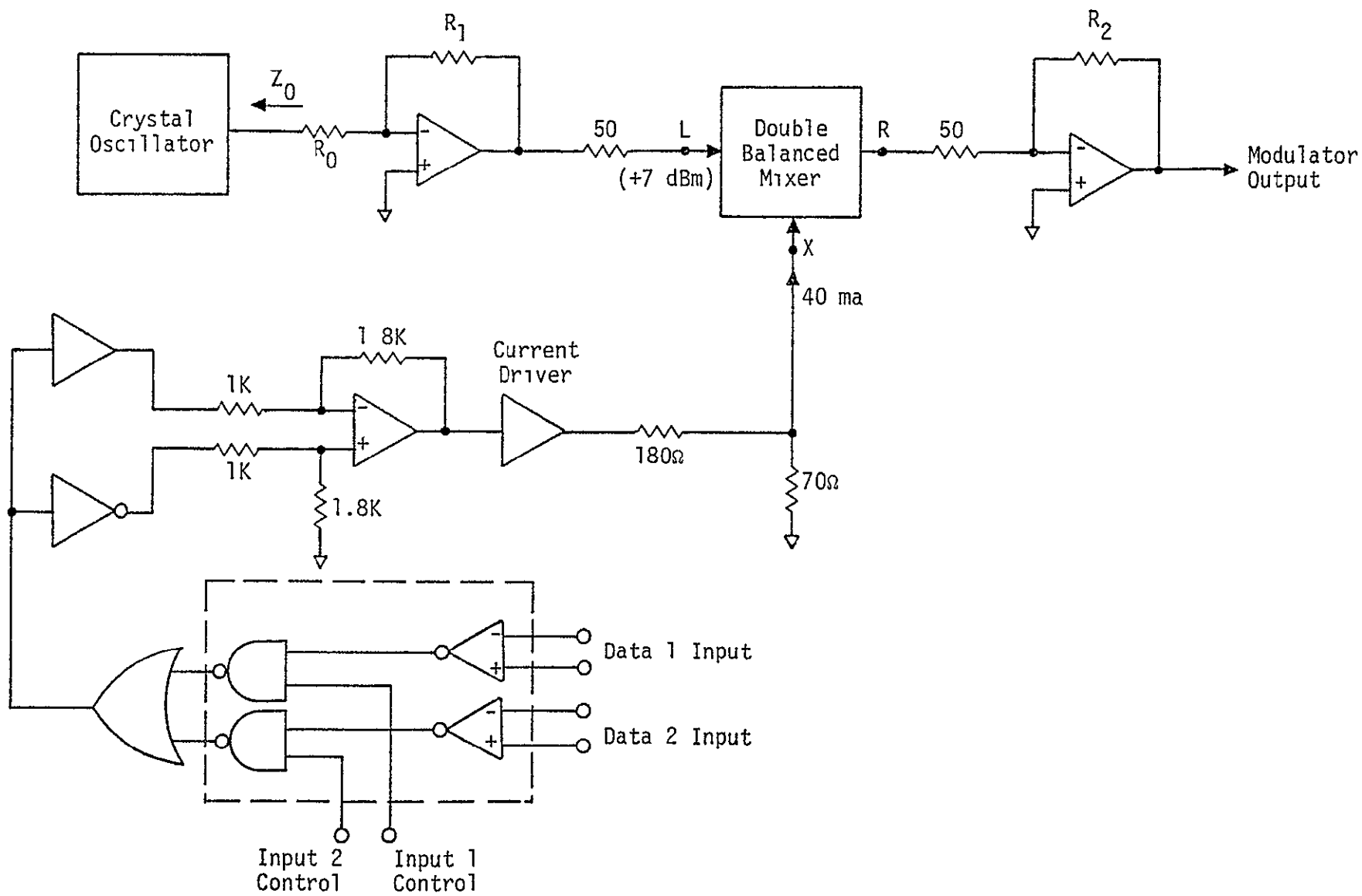


Figure 4-16. Detailed Biphase Telemetry Modulator

be appreciable and (2) the output is some form of periodic pulse waveform whose fundamental must be obtained by a BPF. Custom design, and oftentimes special compensation, is necessary to achieve specified deviations and modulation frequencies. As a result, the use of the MV circuit to satisfy the multiple parameter requirements listed above is untractable.

The translated VCO approach has been selected as the best way to meet the flexibility needed. Figure 4-17 shows a detailed diagram.

The modulation signal is input through a differential amplifier (Burr-Brown 3550J) to remove any common mode components. Gain is designed to establish the proper deviation range to the VCO, and the input resistor R_A is selected to match the modulation source impedance. The lowpass filter following the input amplifier has four selectable 3-dB frequencies—20, 50, 100 and 200 kHz—and is a two-pole operational type (see Section 4.2 of [8] for detailed information).

The LC type VCO operates at a nominal frequency of 2.8333 MHz* and is capable of being deviated up to $\pm 2\%$. In practice, the ± 30 kHz and ± 160 kHz peak deviations require that the VCO be deviated no more than $\pm 1.2\%$, thus assuring good linear operation. Greenray Industries, Inc., produces VCOs which meet the general requirements for the subject application. Their Model PH-230 LC-VCO requires some modification to permit modulation frequencies up to 170 kHz, but it meets all other conditions.

The VCO output is split into two channels by a Merrimac PDM-20-10 hybrid. In the upper channel, called the narrow deviation channel, the VCO output is mixed with a modulation-free reference frequency of 1.1333 MHz.* The reference frequency is generated by a crystal oscillator (Ferwalt Model X045) and split into two outputs by a Merrimac PDM-20-10 hybrid.

The upper channel mixer output is passed to a LPF which retains the mixer difference frequency at its output. This filter is a five-section LC type (K&L Model L53) with a 3 dB frequency of 2.5 MHz. Such characteristics pass the difference frequency and its sidebands with little distortion while providing up to 100 dB attenuation at the sum frequency.

*These frequencies were selected so that intermodulation terms and feedthrough will not fall at the 1.7 MHz output.

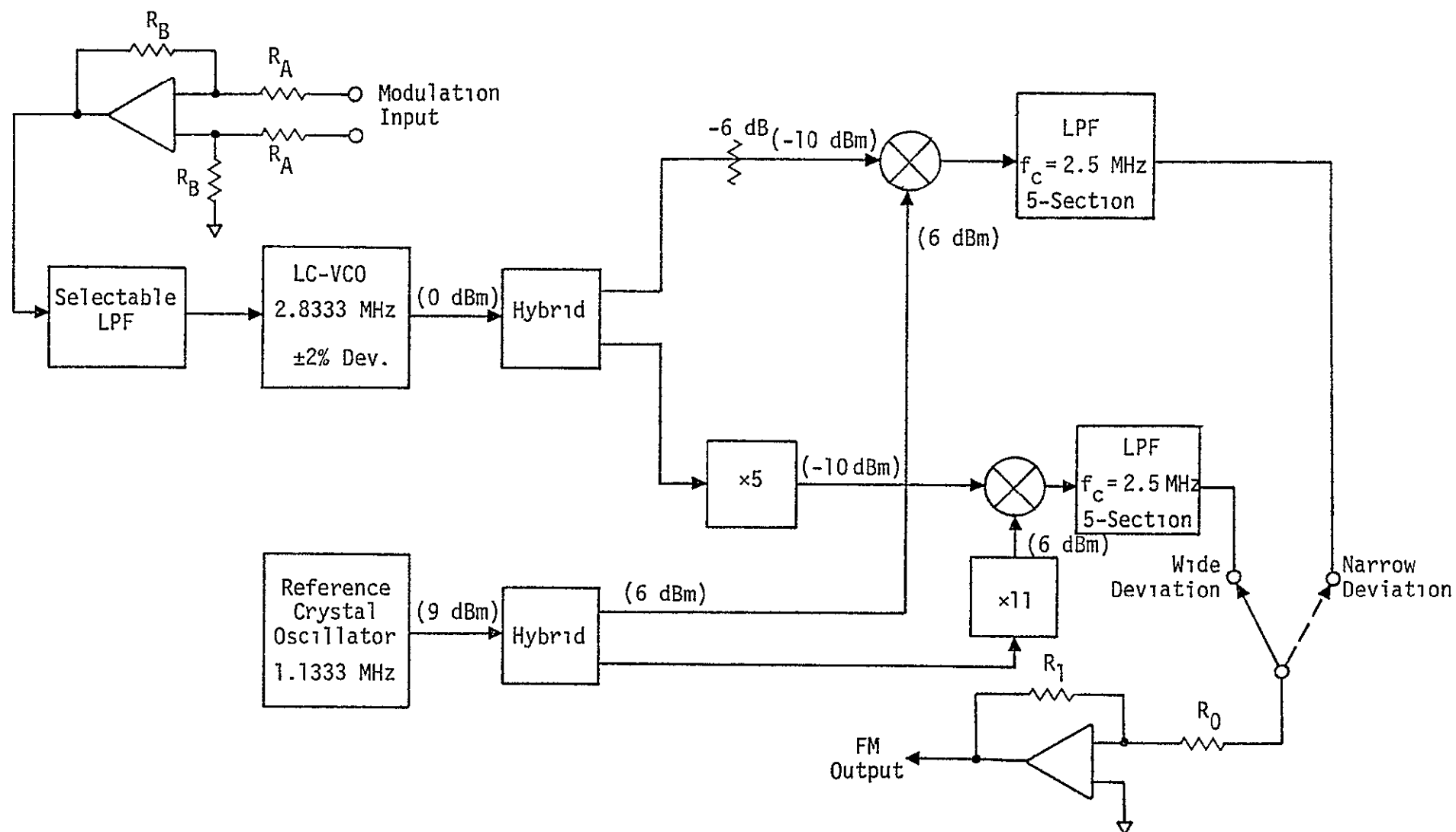


Figure 4-17. Detailed Frequency Modulator

The lower or wide deviation channel operates to multiply the VCO frequency and its deviation by a factor of 5, which is then mixed with the reference frequency multiplied by 11. Again, the difference frequency of 1.7 MHz is selected by a LPF, identical to that used in the narrowband channel so as to provide equivalent frequency transfer characteristics to both channels. The mixers used in both channels are Merrimac Model DMS-2-250.

A selector switch is provided to route either the narrow or the wide deviation channel to the output amplifier. This amplifier has an input resistance to properly terminate the LPF (50 ohms) and a gain sufficient to provide a voltage to the transmitter phase modulator which will permit the maximum deviation required.

4.4 Data Processors and Generators

4.4.1 General Requirements

To provide for realistic evaluation of Shuttle Payload Communication equipment, the payload simulator must be capable of delivering to the Orbiter telemetry data various frame formats at various bit rates. The telemetry frame formats generally depend on the payload and the bit rate used. The bit rates, however, are standardized. For NASA payloads, the range of bit rates extends from 1 kbps to 16 kbps. For SGLS payloads, the bit rates range from 0.25 kbps to 256 kbps*.

Presently the ESTL has a number of types of equipment which can provide telemetry data to the payload simulator unit. During the tests involving the use of the return link of the payload simulator, the ESTL-generated telemetry data is applied to the telemetry modulator(s) of the simulator and then routed to the Orbiter equipment via either a hardware or an RF link.

Depending on the telemetry source used, the Orbiter equipment delivers the telemetry data to either a bit error detector or the 642B computer for bit error rate evaluation. For example, if one of the PCM telemetry simulators, such as Dynatron Inc Model 100, is used as a source of data applied to the telemetry input of the payload simulator, the telemetry output of either the PSP or the CIU can be applied directly to the bit error detector which then provides a measure of bit error rate. In this case, the bit error detector simply compares each telemetry bit received from the Orbiter avionics units with an original bit delivered to the payload simulator input from the PCM simulator.

Because the comparison is on a bit-by-bit basis, only the overall bit error rate is measured and no particular segment of telemetry data is singled out for analysis. When a detailed analysis of bit errors within a specific segment of the telemetry stream is required, the telemetry data output of either the PSP or the CIU unit is applied to the 642B computer. The computer then identifies the particular segment of the data and estimates

*See Table 2-6 for a detailed listing of NASA and SGLS bit rates.

the bit error rate for that selected group of bits. This computerized analysis of specific bits within the telemetry stream provides the ESTL with a capability to perform command verification.

The capability for verifying the reception of a proper command by the payload is a definite requirement for certain payloads, the IUS being one of them. Such verification is typically implemented by sending the command which is received and detected by the payload back to the command source via the telemetry link.

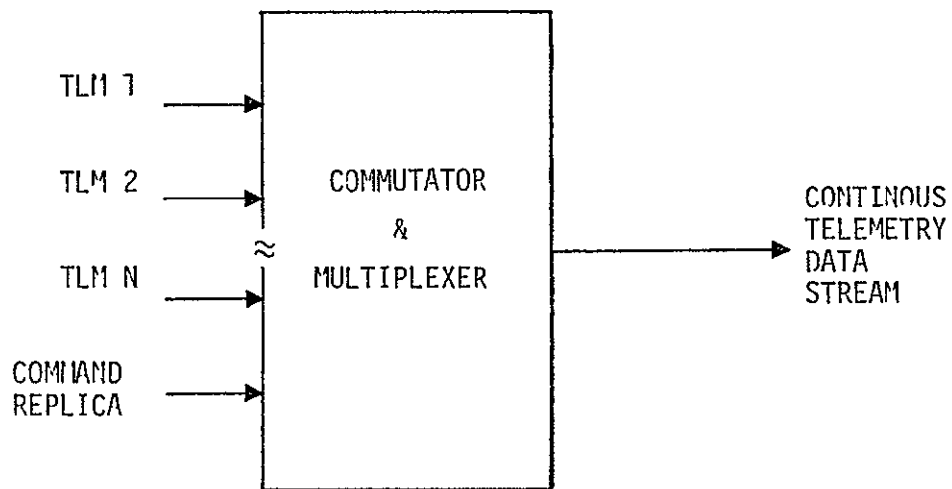
Consequently, the payload simulator must provide the capability for multiplexing the payload received commands with the payload telemetry data. The associated constraint, however, is the minimization of the multiplexer complexity. Proposed approaches for multiplexer implementation are described below.

Another requirement for the data generator equipment of the payload simulator is that of providing a high rate (up to 50 Mbps) sequence which is characteristic of the Spacelab telemetry multiplexer output. This function, however, can be performed by off-the-shelf equipment such as the HP Model 8018A 50 Mbps Serial Data Generator or an equivalent unit.

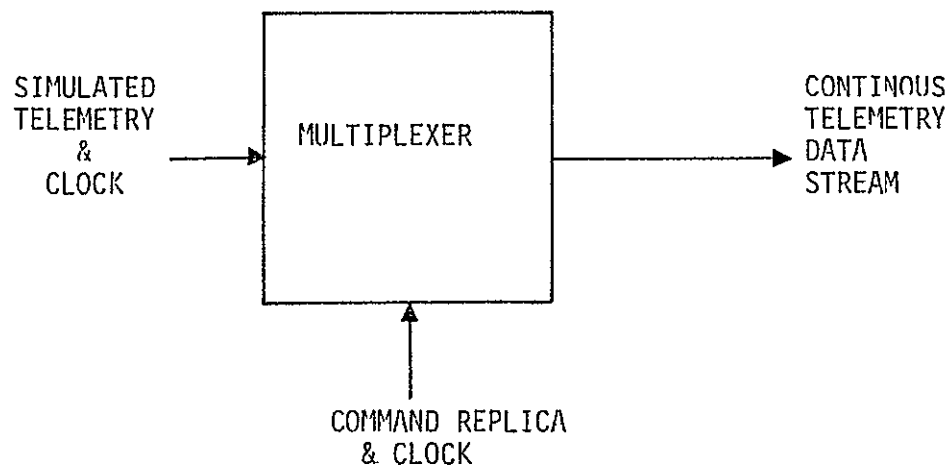
4 4.2 Generic Description

Figure 4-18 shows a generic block diagram for two kinds of telemetry multiplexers. Part (a) of this figure is a configuration which is similar to that of a conventional telemetry multiplexer employed by a typical payload. As shown, several telemetry inputs (1 through N), including a command input, are applied to the multiplexer. Within the multiplexer, these inputs are sampled by a commutator and are multiplexed to form a telemetry frame of a predetermined format. The communication sequence and rate determine the location and the number of bits each telemetry signal source occupies within a single telemetry frame. The commutation is determined by an internal clock and submultiples thereof.

In comparison, the generic simulator telemetry multiplexer, such as shown in part (b) of Figure 4-18, does not require commutation because the simulated telemetry data is already a continuous bit stream clocked at a selected telemetry rate. This bit stream is composed by software commutation of preprogrammed words to simulate the various input signal



(a) Generic Conventional Telemetry Multiplexer



(b) Generic Simulator Telemetry Multiplexer

Figure 4-18. Generic Configurations for (a) Conventional and (b) Simulator Telemetry Multiplexer

bit groups. Note also that a telemetry clock is available along with the simulated telemetry data. This clock can then be used to multiplex the command replicas with the telemetry data.

Because the command bit rate is typically much slower than the telemetry bit rate and since the commands occupy only a fraction of the commands data stream, the command data can be easily fitted into a typical telemetry frame. The function of the multiplexer is then reduced to a temporary storage of commands and their insertion into the appropriate slots of the telemetry stream. Thus, the commutation in this case is minimal.

4.4.3 Functional Description

A functional block diagram for the telemetry multiplexer of the payload simulator is shown in Figure 4-19. Briefly, the multiplexer operates as follows. The telemetry data from the PCM simulator is applied to the multiplexer according to a predetermined frame format but with the slots to be filled by the command replica bits set to zero. Prior to the insertion of the command bit, the telemetry data is simply passed through the multiplexer to the telemetry modulators.

At the same time, the serial command data stream developed by the CDU is applied to the command detection unit. This unit recognizes the end of the command preamble and also the end of other words preceding the command. The signal indicating the onset of the command word transfers the proper command bits to the command storage shift register. After this transfer, the command replica bits are ready for clocking into the telemetry stream.

The sequence of transferring the command replica bits to the telemetry stream is initiated by a frame sync pulse. The location of this pulse can be programmed to occur at any one of the positions occupied by the bits comprising the telemetry frame sync word. Because the location of the command replica words is known with respect to the frame sync pulse, a counter enabled by the sync pulse and driven by the telemetry clock determines the time at which the serial transfer of the command data bits must be initiated. In this way, the replica command bits are clocked into the proper slots of the simulated telemetry stream. Upon completion of

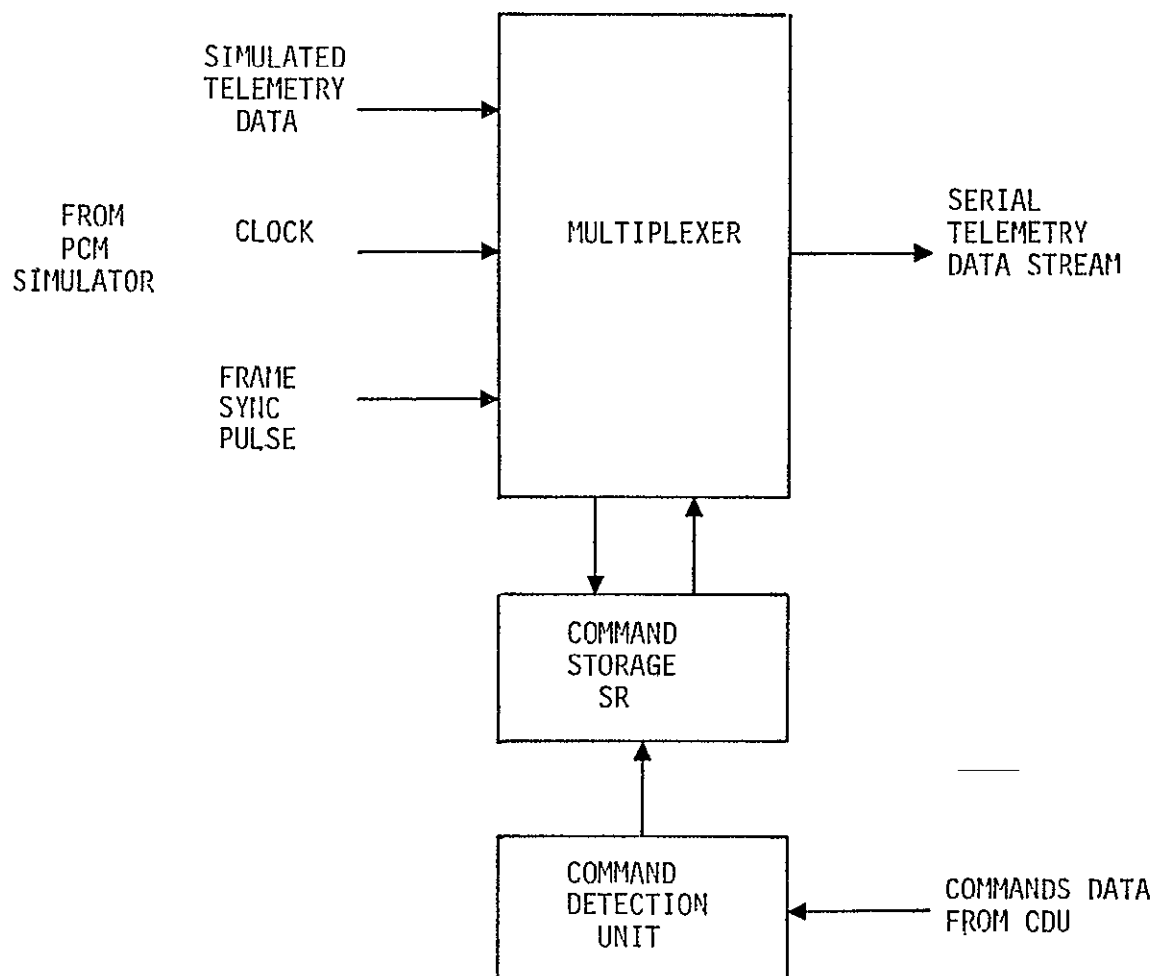


Figure 4-19 Functional Block Diagram for Payload Simulator Telemetry Multiplexer

the command replica bit transfer, the remaining bits of the simulated frame are passed on to the output of the multiplexer.

4.4.4 Detailed Implementation of Telemetry and Commands Multiplexer

4.4.4.1 Introduction

The detailed description of the implementation of the telemetry and command data multiplexer is presented in this section. To provide concreteness to the implementation described, the telemetry and command formats employed by the IUS are used. The proposed scheme can, of course, be applied to other types of payloads.

4.4.4.2 Telemetry Format

Of particular interest to the payload simulator functions is the ability to handle the IUS telemetry characteristic of the RF link. The telemetry frame format [10] used by both DOD and NASA for the IUS/Orbiter RF link is shown in Figure 4-20. The quantitative characteristics of this link are as follows:

Bit Rate	16 kbps
Bits/Word	8
Words/Main Frame	80
Bits/Main Frame	640
Frame Rate	25 Main Frames/Second

As shown in Figure 4-20 there are three consecutive 8-bit words assigned to each command replica word within each main telemetry frame. Thus, the maximum rate at which the command bits can be multiplexed into the telemetry stream is

$$\begin{aligned}\text{Maximum Command Mux Rate} &= \frac{\text{words}}{\text{frame}} \times \frac{\text{bits}}{\text{word}} \times \text{frame rate} \\ &= 3 \times 8 \times 25 = 600 \text{ bits/sec.}\end{aligned}$$

The maximum sustained command rate for this link is 12 words per second, each word being 8 bits long. Thus, the sustained command bit rate is 96 bits/second, a number well within the capability of the telemetry link. It must be noted here that the nominal "command" bit rate for the Orbiter/IUS RF link is 1000 kbps. This means that only about 10 percent of the bits

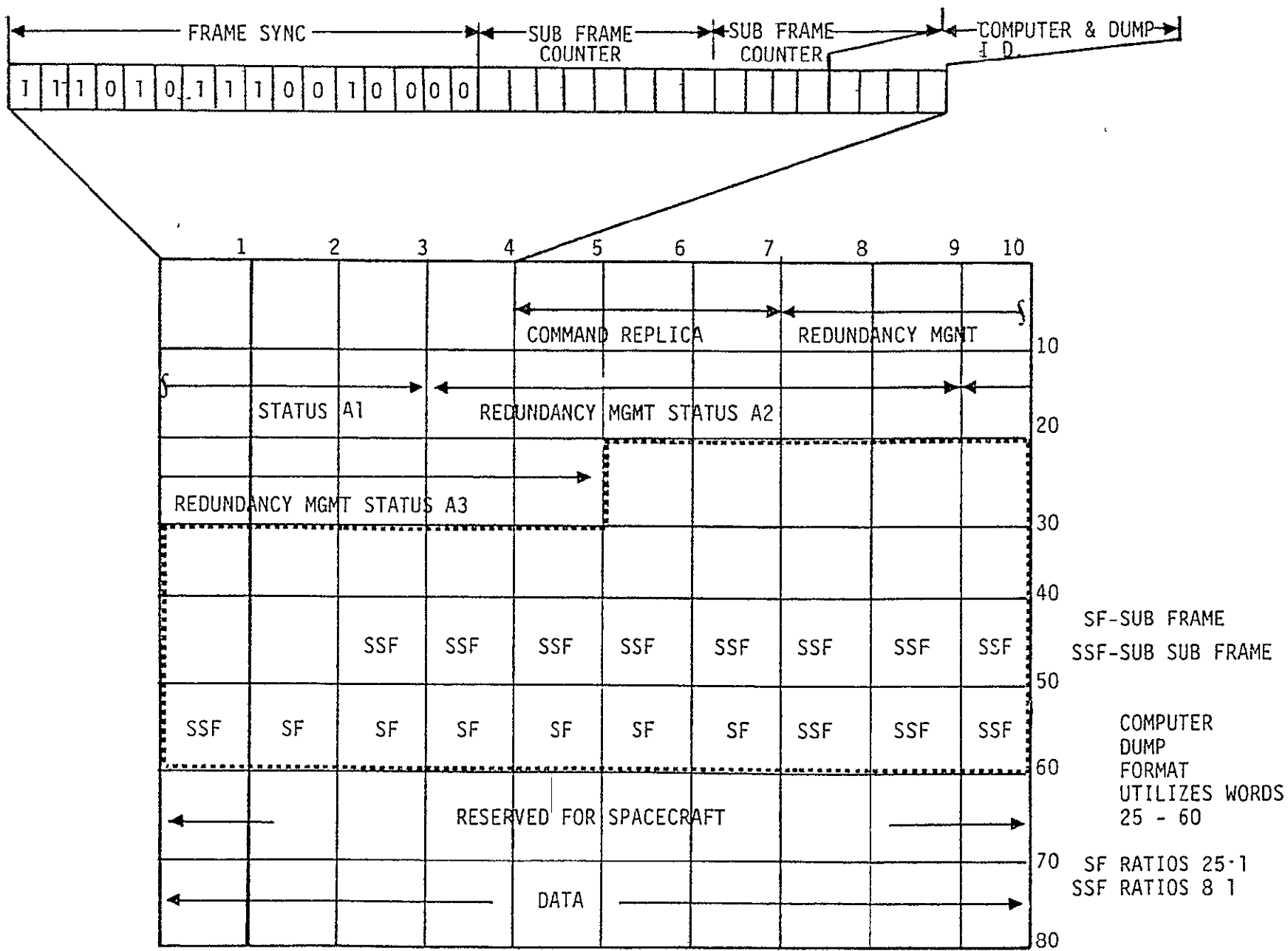


Figure 4-20 TELEMETRY FORMAT DESIGN - (DOD/NASA)

received and processed by the CDU are actual command bits. The remainder of the bits in the command stream are used for preambles, postambles and idle fill-in patterns.

4.4.3 Command Formats

The command system of the IUS is designed to handle the following three formats: (1) NASA, (2) DOD Clear Text, and (3) DOD with authentication [10]. The format for a single NASA command is shown in Figure 4-21. The DOD command formats are shown in Figure 4-22. As seen in Figure 4-21, the preamble for NASA single commands consists of 128 alternating 1's and 0's. Consequently, the end of the alternating pattern indicates the beginning of an ambiguity word followed by an address word, which is then followed by a 20-bit command.

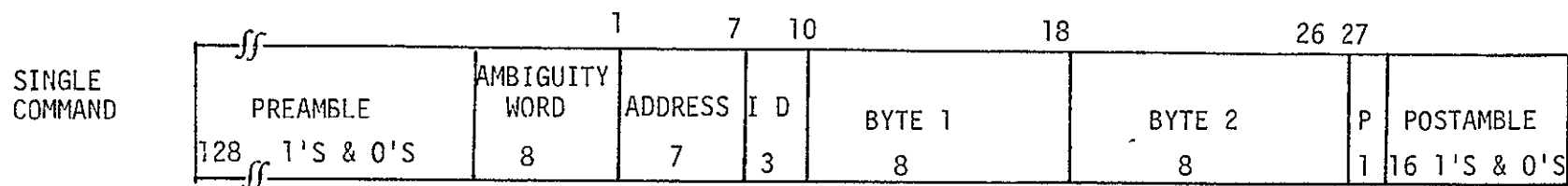
For the DOD formats, the end of the preamble is indicated by the termination of a continuous S-bit stream which is at least 16 bits long. Thus, an \overline{S} signal and an indication of "16 continuous S's in store" indicates the beginning of either the clear test or the authentication command pattern.

The preambles of both NASA and DOD commands contain sufficient information to initiate the counter which then will indicate the start of the 20-bit sequence representing the command information.

4.4.4 Command Replica Format

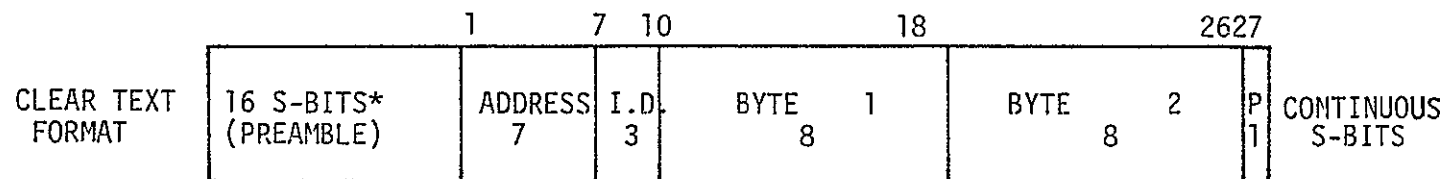
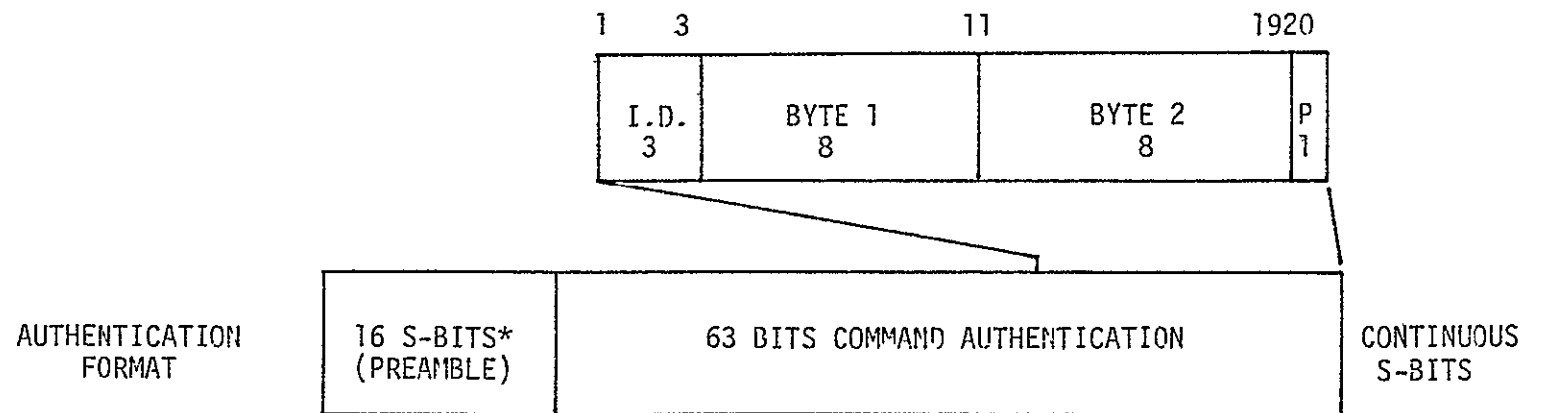
The command replica format for the IUS/Orbiter telemetry link consists of 24 bits, 20 of which are replicas of the command itself, the remaining four are generated by the payload (in this case, IUS) data processing subsystem. Figure 4-23 shows the clear text command replica word used by both DOD and NASA telemetry links.

With the payload simulator in the command verification loop, the last four bits in the replica word have no significance because no processing of the command structure is done by the payload simulator. It is therefore logical to suggest that "1" always be placed in the "accept" and "executed" bit positions (21 and 23), a "0" into the "reject" position, and either a "1" or a "0" in the last bit position (Bit 24).



COMMAND WORD STRUCTURE COMMON TO CLEAR TEST SGLS
 2 KBPS RATE ON 16 KHZ PSK SUBCARRIER
 12 WORDS/SEC SUSTAINED (16 KBPS TLM)

Figure 4-21. NASA Command Format Design



*MINIMUM

1 Kbps RATE ON TERNARY FSK SUBCARRIERS	
AUTHENTICATION	(63 BITS - 20 BIT COMMAND WORD)
CLEAR TEXT	(27 BIT COMMAND WORD)
5 WORDS/SEC	(AUTHENTICATION 16/64 Kbps TLM)
12 WORDS/SEC	(CLEAR TEXT 16 Kbps TLM)

Figure 4-22 DOD Command Format Design

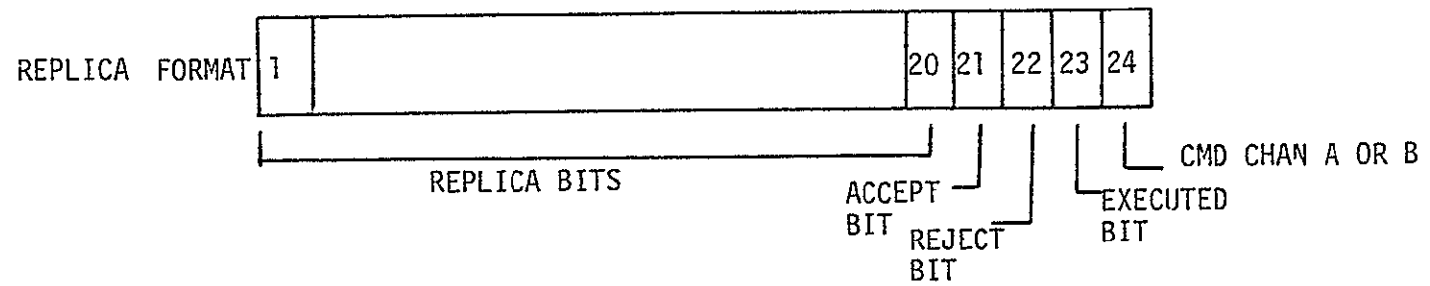


Figure 4-23. Clear Text DOD/NASA Command Replica Word Format

An alternate approach for the NASA mode would be not using bits 21 through 24 at all and allowing the command verifier, which in this case will be the 642B computer, to examine only the replica bits 1 through 20.

4.4.4 5 Multiplexer Implementation

Using the implementation philosophy for a multiplexer to be used with the payload simulator for the commands verification presented in the preceding paragraphs, the architecture of such a multiplexer as shown in Figure 4-24 can be described.

Consider first the command recognition subsection of the multiplexer. This subsection is comprised of. (1) preamble end detector, (2) ambiguity (or address) word detector and (3) command clock counter.

The preamble end detector recognizes either the end of a 128-bit sequence of alternating ones and zeros (NASA mode) or the end of a 16-bit long S-bit sequence (DOD clear mode). The detector then provides an "examine data" pulse to the A-word detector, the "A" standing for either the ambiguity word or the address word. The structure of these words is known a priori, and thus the detector can be programmed to recognize these words. The "examine data" pulse then also starts the command clock counter. If either one of the A-words is detected, the "A-detect" pulse is issued to the command clock counter. This pulse is "anded" with a "decoded-7" pulse out of the counter. The resultant pulse triggers the "7 to 27" bit pulse. The "7 to 27" pulse opens gates AG_1 and AG_2 ; thus, the 20 bits comprising the command are entered into the command store SR at the command rate. The $\overline{7 \text{ to } 27}$ signal applied to AG_3 prevents the telemetry clock from interfering with the transfer of the commands to the storage SR.

Upon the termination of the "7 to 27" pulse, the $\overline{7 \text{ to } 27}$ signal goes to "1," thus enabling one of the inputs to gate AG_3 . The enabling of gate AG_3 takes place when the "16 to 36" pulse is presented at the output of the telemetry clock counter. The latter counter is actuated by the frame sync pulse provided by the PCM simulator. For the case shown, this frame sync pulse appears at the last position of the frame sync sequence. Thus, the counter has to count the 16 pulses occupied by the sub-frame counter and "Computer and Dump I.D." pulses (see Figure 4-20).

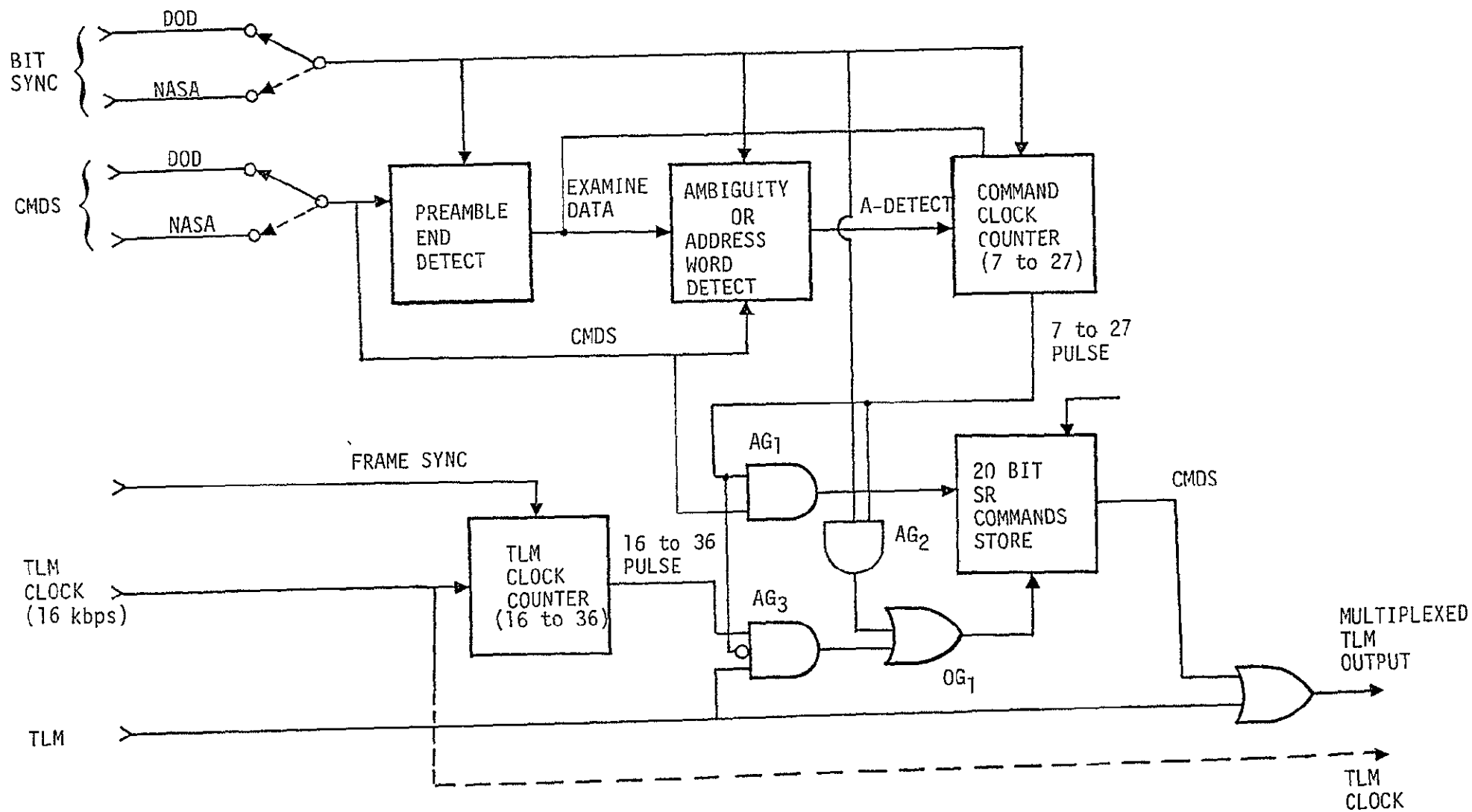


Figure 4-24. Telemetry/Commands Multiplexer Functional Block Diagram

The "16 to 36" pulse then clocks the stored 20 command replica bits into the empty places of the telemetry stream. If one were to utilize all 24 bits available within the telemetry frame, then the telemetry counter output pulse would be changed to a "16 to 40" duration and the four artificial bits would then be supplied from the preassigned position of a 24-bit command store register

The example presented above applies only to clear text commands of both NASA and DOD formats. In the authentication mode, special equipment, such as encryptors and decryptors, must be included in the link. The replica information provided by the decryption equipment to the multiplexer consist of two words. One of these words is the command replica identical to the clear text version. The second word is the variable control counter (VCC) word. These two words are inserted alternately into the telemetry stream for commands replica verification. The formats of these two words are shown in Figure 4-25. The transfer of these words into the command storage shift register prior to multiplexing must be aided by the KIR-23 decryptor. For technical details concerning this interface, see [11].

4.4.4.6 Multiplexer Function in Payload Link Testing

Figure 4-26 shows the functional block diagram for NASA mode testing of commands verification. It also shows how the multiplexer can be bypassed to provide testing of only the telemetry data transmission (i.e., telemetry without commands).

Consider first the block diagram of Figure 4-26 with the switches in position (1). This condition corresponds to the commands verification mode. The commands are generated by the 642B computer and transferred via the parallel-to-serial interface to the PSP. From the PSP the commands are transmitted to the transponder by means of the PI.

At the transponder the simulated commands are applied to the NASA CDU which then recovers the clock and applies both the commands and the clock to the telemetry multiplexer. This multiplexer also receives the telemetry data, telemetry clock and the frame sync signals from the PCM telemetry simulator*

* Dynatron Inc, Model 100

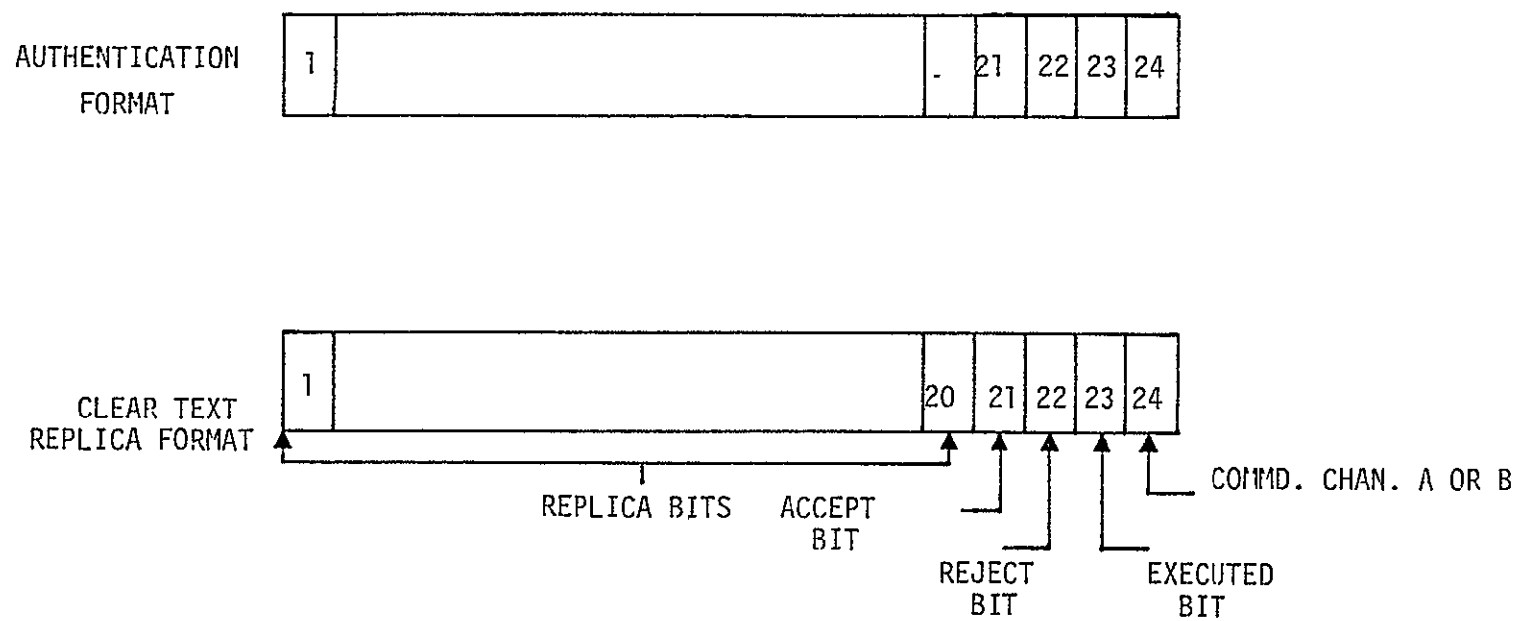


Figure 4-25. Command Replica Word Format (DOD)

The multiplexer thus performs as described in the preceding paragraphs. The combined telemetry-plus-commands signal is fed to the telemetry modulator and then to the RF output of the transponder. After being picked up by the receiver of the PI unit, the telemetry data is applied to the PSP where it is demodulated and its clock recovered. The telemetry data is then applied via the serial-to parallel interface to the 642B computer where it is analyzed for the validity of the returned command bits. The arrival at the 642B computer of the commands embedded in the telemetry stream completes the commands verification loop.

If only the testing of the telemetry link is required, the switches of the block diagram shown in Figure 4-26 are placed in position (2). This results in bypassing the multiplexer and delivering the telemetry stream to the bit error detector instead of the 642B computer. The command verification testing for the DOD clear text mode is shown in Figure 4-27. The configuration shown is very similar to that of the NASA configuration with the exception that a CIU is used instead of the PSP to interface with the PI. Also, since at this time it is not known whether a clock will be available at the CIU output, the clock supplied by the PCM simulator is used for transferring the telemetry output across the serial-to-parallel interface to the input of the 642B computer.

4.4.5 Alternate Method for Telemetry and Commands Multiplexing

The capability of the Dynatronics Inc., Model 100 PCM telemetry simulator to alter all of the bits of its output format under the control of an external input presents an opportunity to use this simulator as the telemetry multiplexer. With this approach a separate telemetry multiplexer unit is not required in the payload simulator. Figure 4-28 shows the functional block diagram for implementing such an alternate multiplexer scheme. The block diagram shown is for the SGLS/DOD mode, but in principle it is identical to that for the NASA mode with the exception of the PSP playing the role of the CIU.

The salient feature of the block diagram shown in Figure 4-28 is that the commands and clock developed by the CDU are applied back to the 642B computer where they originated. The commands are returned to the 642B computer via an additional serial-to-parallel interface. The delivery of

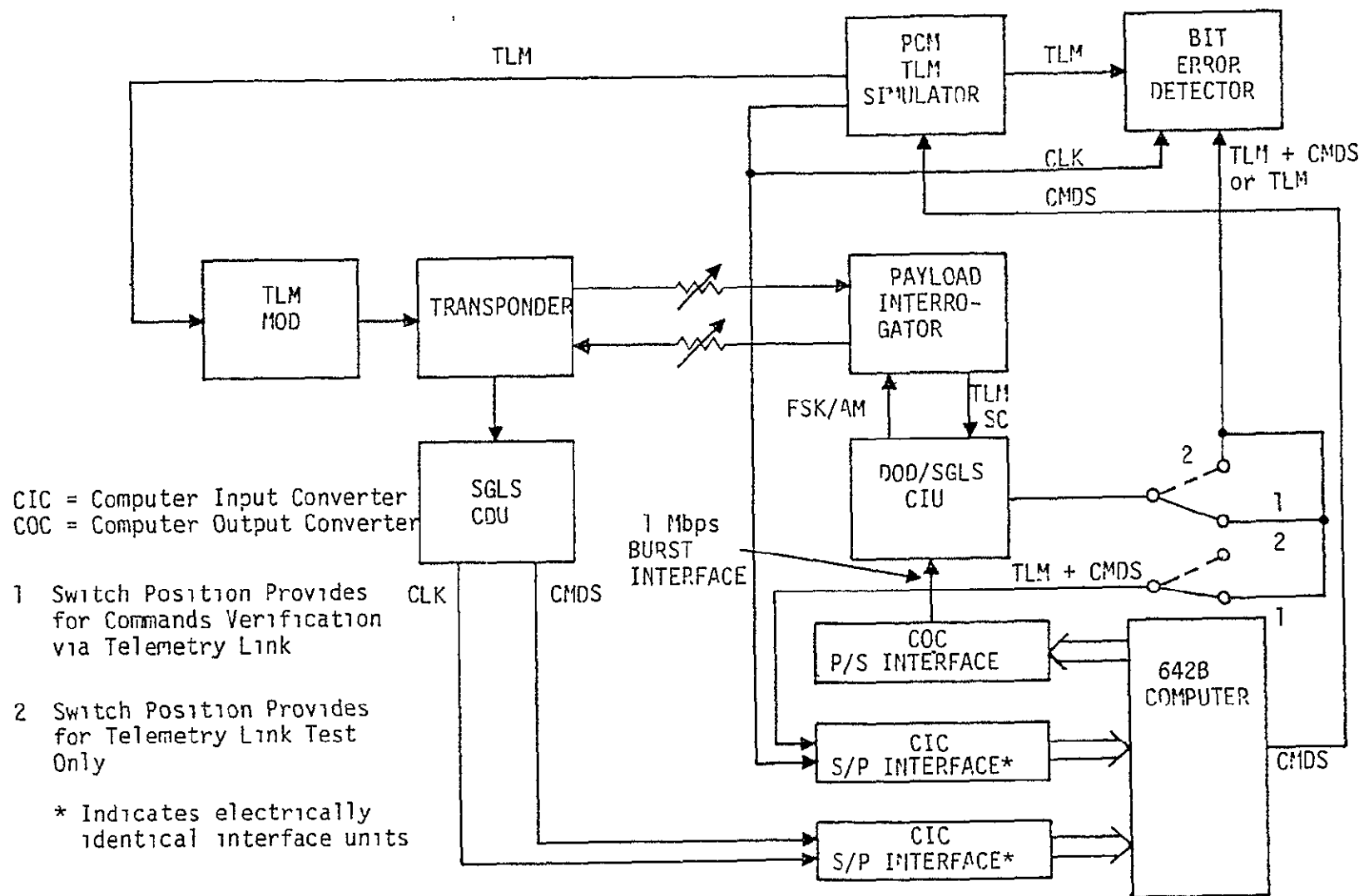


Figure 4-28 Alternate Command Multiplexing Scheme User PCM Simulator as Multiplexer

the commands and the accompanying clock is via cables which are a part of the payload simulator setup.

The computer analyzes the command stream and selects the twenty bits comprising the command replica and sends them to the PCM telemetry simulator. The computer may also supply the additional four bits to complete the 24-bit command verification word.

The composite telemetry stream is then applied to the telemetry modulator and the transponder for transmission to the payload interrogator. This telemetry stream, of course, has now the command verification information included at the proper place within the telemetry frame.

The composite telemetry stream is also applied via a second serial-to-parallel interface unit back to the 642B computer. The computer examines the telemetry stream and recovers the commands which are used for the final command verification.

Note that with this scheme the commands pass twice through the computer. The first time they arrive at the relatively low command rate. The second time they arrive at the relatively fast telemetry rate. Also, the first time there are only 20-bits in the command replica, and the second time there are 24-bits, the additional four bits being provided by the computer during the first passage.

The advantages of this alternate scheme are (1) elimination of a separate multiplexer unit, (2) increased capability for handling various command formats (only a software change is required to alter formats), and (3) expanded capability for testing the bit error rates of both the telemetry and command links simultaneously.

The disadvantage is that an additional serial-to-parallel interface unit is required to provide the simultaneous supply of serial command and telemetry data to the 642B computer. One could consider, of course, a time-multiplexed serial-to-parallel interface to handle the command and telemetry data simultaneously. The additional equipment required in either case for this alternate approach is about the same complexity as a separate multiplexer which it replaces.

4.4.6 High Rate Data Generator

The Spacelab payload will generate a data stream which may be delivered to the Orbiter at rates of up to 50 Mbps. This data will be delivered over a hardwire only. At the Orbiter, this data will be applied to the Ku-Band Signal Processor Assembly where it will be rate 1/2 encoded. The encoded data stream will then be transmitted on the Ku-band link via the TDRS to the ground.

One of the requirements imposed on the TDRS users is that
"....the transition density of the data stream shall average
64 transitions in 512 bits, with a maximum separation of 64
bits between successive transitions... "

At the present time the data transmission statistics of the Spacelab multiplexer are not defined. It is reasonable to postulate, however, that they will vary from a random data, approximated by a pseudorandom sequence, to that of a quasi-structured stream within the constraints imposed by the TDRS usage.

A reasonable and cost-effective solution is to use commercially available equipment possessing sufficient flexibility to structure the variety of data formats. A likely candidate for such equipment is the Hewlett Packard Model 8018A Serial Data Generator. This generator has a programmable memory which can produce data frames of up to 2048 bits, with each bit being programmable. In addition, pseudorandom binary sequences of length $2^n - 1$, with $n = 9, 10, 15, 20$, can be produced. This equipment can also interleave words extracted from the 2048 bit memory with portions of a pseudorandom sequence. Such features provide for simulation of a preamble, data message, and a postamble.

Other high rate data simulators which may be available to the ESTL may be substituted for the 8018A model provided that they meet the requirements of the function to be simulated.

4.5 Computer Interface Equipment

4.5.1 General Description

The Univac M642B computer is a key element in the support of the Orbiter avionics testing via the Payload Simulator equipment. This computer is used to generate simulated commands which, after passing through the avionics equipment and payload simulator, are fed back to the computer for verification and bit error count. The 642B computer is also used for telemetry data bit error count. The PCM simulator generates the telemetry which reaches the computer via the payload simulator/avionics equipment link. Furthermore, the 642B computer can recognize certain bit patterns within the telemetry stream and perform bit error rate determination based on the errors within these patterns. This capability is particularly useful for testing the command verification function where the command replicas are multiplexed with telemetry data. During such tests the computer generates simulated commands and subsequently recovers them from the telemetry stream for error analysis.

The input and output interfaces of the 642B computer require parallel data formats. The input and output interfaces of the Orbiter avionics and of the payload simulator, however, require serial data. Consequently, interface equipment providing both the serial-to-parallel and the parallel-to-serial conversion is required for the payload simulator test setup.

Functionally, the interface equipment is divided into two units: (1) equipment which supplies data to the computer and (2) equipment which delivers the simulated data from the computer to the avionics and payload simulator subunits. In this report, these two units will be referred to as the Computer Input Converter (CIC) and the Computer Output Converter (COC), respectively.

The function of the CIC is to feed the serial data supplied by the CDU (commands), the PSP (telemetry) and the CIU (telemetry) to the 642B computer for statistical analysis. Consequently, the CIC is a serial-to-parallel converter.

The primary function of the COC is to supply the simulated commands from the 642B computer to either the PSP or the CIU equipment. For payload simulator testing the COC also provides command data directly to the CDU. Because these units accept serial data, the COC is a parallel-to-serial converter.

The secondary function of the COC is to control the configuration of the PSP. The control requires that the status of the PSP be available to the computer. The PSP status reporting requires that the serial data from the PSP be converted to a parallel format for transmission to the computer. Consequently, the COC also has a serial-to-parallel conversion capability. This capability, however, is for auxiliary housekeeping only.

4.5.2 Computer Input/Output Protocol

Before proceeding with the detailed description of the CIC and the COC equipments it is advantageous to present the description of the input/output protocol used by the 642B computer for interfacing with its peripheral equipment (PE). Figure 4-29 shows the control signals involved in the 642B/peripheral equipment interface. Table 4-6 provides the explanation of these signals.

4.5.3 Computer Input Converter

4.5.3.1 Generic Description

Figure 4-30 shows a generic block diagram of a serial/parallel data converter unit. The input to the interface is a stream of serial data and its clock. The availability of the serial data clock eliminates the requirement for generating this clock from the incoming data.

The serial data arrives at the data converter in a continuous, uninterrupted stream. Parallel data is shifted out in N-bit words at a different rate. The requirement for buffer storage of the incoming data is minimized when the following condition is met:

$$\text{Parallel Rate} \geq \frac{\text{Serial Rate}}{N}$$

where N is the number of bits in the parallel word. For this condition, the size of buffer storage is equal to N.

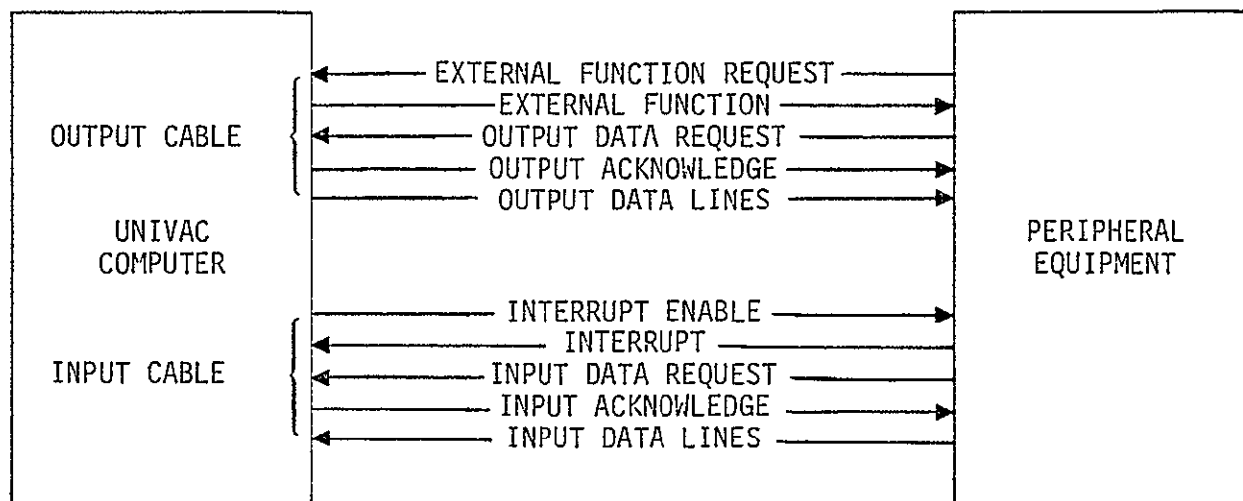


Figure 4-29. Computer-to-Peripheral Equipment Interface

Table 4-6 Control Signals Used for
Input/Output Protocol of 642B Computer

	Signal Name	Origin	Meaning
Input Channel	Interrupt Enable (IE) (642B)	Computer	The computer has enabled its input section to receive an Interrupt signal from the PE.
	External Interrupt (INT)	Peripheral Equipment	Interrupt from the PE is ready for the computer to accept.
	Input Data Request (IDR)	Peripheral Equipment	Data word is on the PE output lines ready for the computer to accept
	Input Acknowledge (IA)	Computer	The computer has sampled the PE data lines
Output Channel	Output Data Request (ODR)	Peripheral Equipment	The PE is ready to accept a computer word
	Output Acknowledge (OA)	Computer	The computer has placed a data word on the data lines, the data lines must be sampled.
	External Function Request (EFR)	Peripheral Equipment	The PE is ready to accept an External Function message on its lines.
	External Function (EF)	Computer	The computer has placed an External Function message on the data lines; the data lines must be sampled

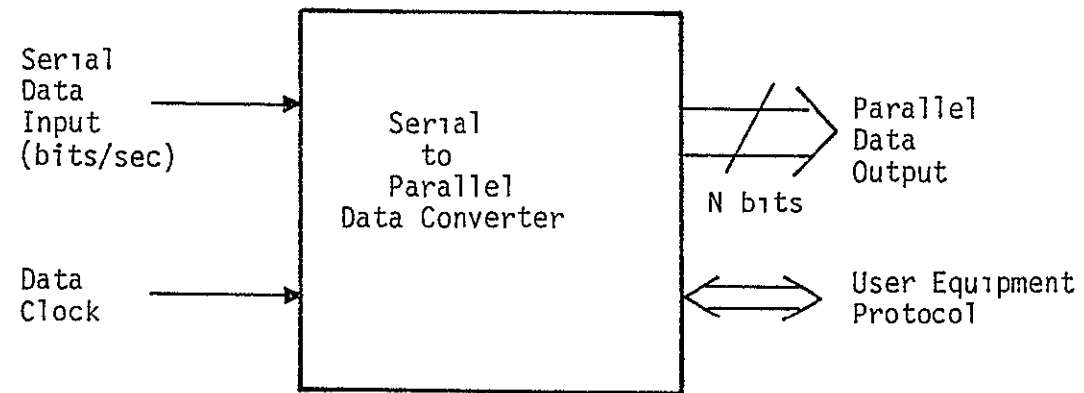


Figure 4-30 Serial/Parallel Data Interface Generic Block Diagram

4.5.3 2 Functional Description

A functional block diagram of the CIC is shown in Figure 4-31. As shown in the figure, the input of this interface can be switched to accept any one of the following serial signals:

- (1) CDU (NASA or SGLS) commands
- (2) PSP telemetry data
- (3) CIU telemetry data

Each of the input data streams are accompanied by their respective clocks. The data clocks not only provide for the serial input of the data but they also determine the timing of the serial-to-parallel (S/P) conversion.

The S/P conversion sequence is initiated by the serial data being clocked into the serial register. The data clock applied to the Timing/Control (T/C) logic initiates a count of the data bits clocked into the serial register. When the count reaches a predetermined number, an S/P transfer command is applied to the S/P conversion unit. This unit transfers the contents of the serial buffer to a parallel holding register. The actual transfer takes place within an interval which is short compared to the duration of the data bit applied to the converter.

Following the S/P conversion epoch, the T/C logic generates a Buffer Transfer pulse. This pulse performs the parallel transfer of the N parallel stored bits to the Data Output Buffer.

The T/C logic also sends an interrupt signal to the computer to initiate the data transfer. The function of this signal is to let the computer logic know that the output buffer is loaded and a word of parallel data can be transferred to the computer from the CIC.

To transfer the parallel data word to the computer, the following protocol sequence is executed by the T/C logic of the CIC:

- (1) The Interrupt Enable (IE) line is sampled
- (2) If the IE line is high, the External Interrupt (INT) line goes high; otherwise, the control logic waits for the IE line to rise.
- (3) When the Interrupt Acknowledge (IA) signal is received, the Input Data Request (IDR) line to the computer goes high.

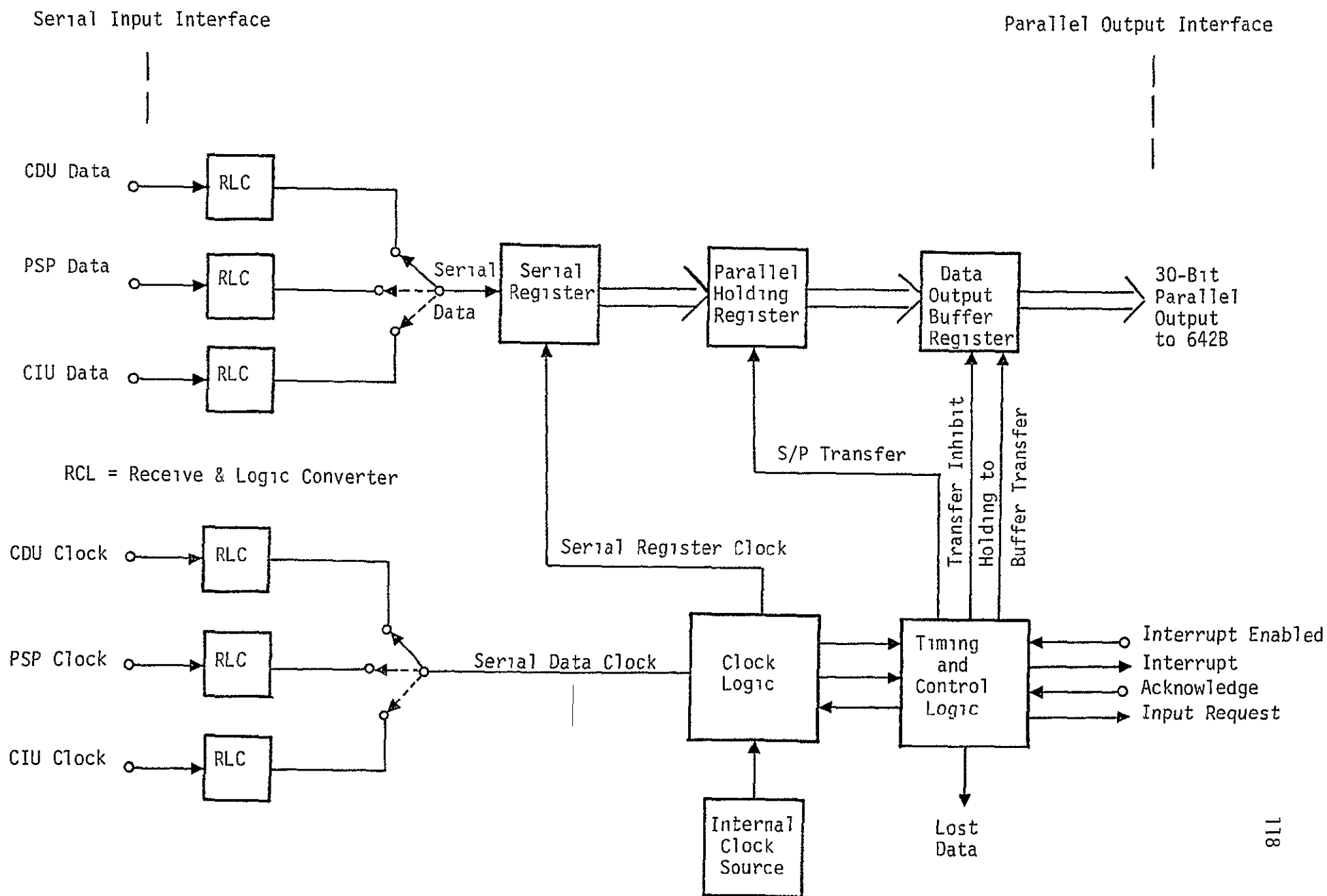


Figure 4-31. . Computer Input Converter Functional Block Diagram

- (4) The computer detects the IDR at the next opportunity.
- (5) The computer samples the Parallel Data Register lines (Input Data Lines).
- (6) The computer raises the Input Acknowledge (IA) line, indicating that it has received the data.
- (7) The CDU interface control logic senses the IA line and drops the INT and IDR lines.
- (8) When the parallel data register contains new data; the process is restarted at step 1).

During the parallel data transfer cycle, the content of the output register should not be changing. The inhibit pulse generated by the control logic is used to perform this function. This pulse isolates the output stages from the intermediate buffer stages which may be receiving the incoming data.

In addition to the input data clock signal, an internal clock is used in the interface for the purpose of synchronizing all the storage and the logic operations within the CIC unit itself.

4.5 3.3 Implementation

The implementation architecture of the serial/parallel interface can take various forms, depending on the logic type selected and designer preference. The important consideration is, however, that all the input and output interfaces are compatible with their corresponding signals and that the computer/peripheral equipment protocol is properly executed.

Considering the data rates handled by the CIC, TTL devices of the 7400 series appear to be a reasonable choice for the implementation of this equipment. Specifically, the lowest rate of the input signal is 8 bps (NASA commands) and the highest is 256 kbps (SGLS telemetry). Assuming that the internal clock may be an order of magnitude higher than the highest input rate (i.e., about 2.5 MHz for the case of 256 kbps), all clock rates are well within the capability of the TTL devices.

Figure 4-32 shows an implementation block diagram for the CIC. As shown in the figure, both the data and the clock inputs are applied to line receivers and line converters to TTL levels.

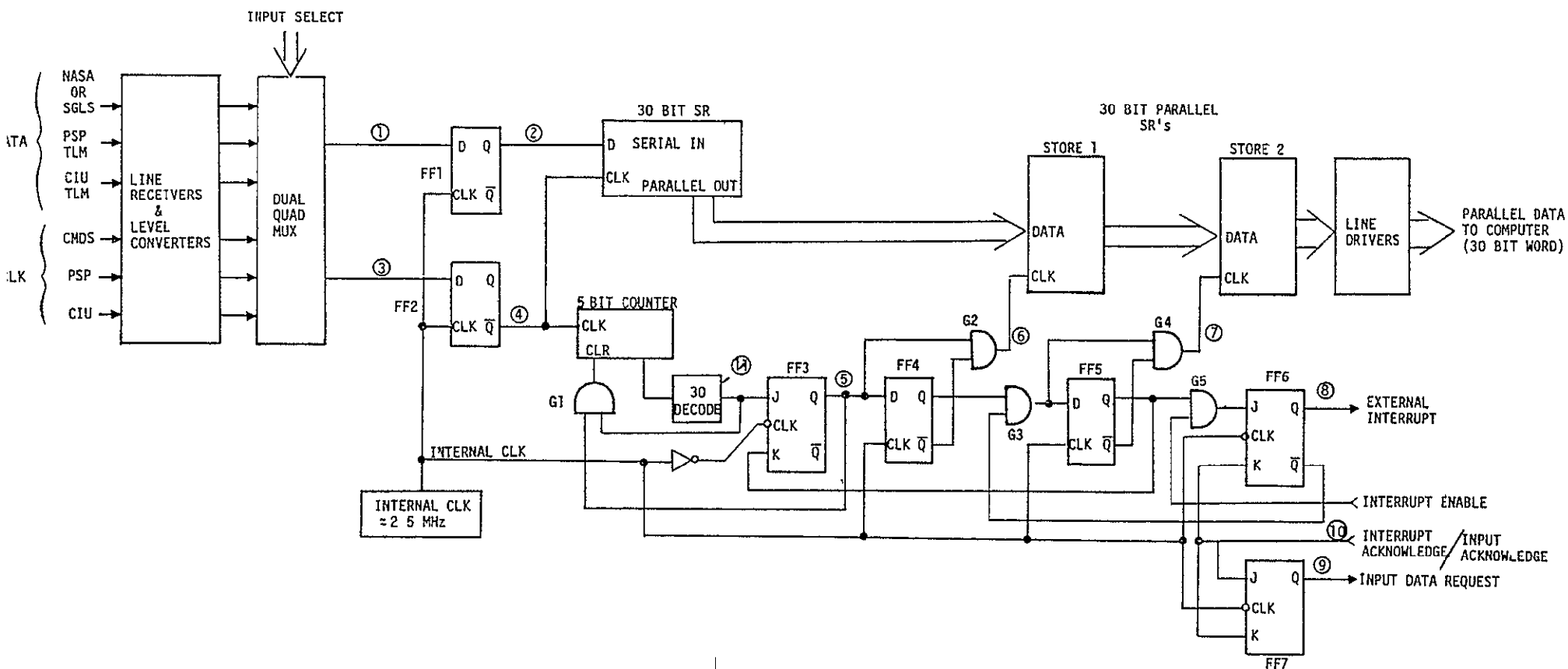


Figure 4-32 Computer Input Converter Implementation

The multiplexer which follows the level converters selects one of the three serial input signal and clock pairs indicated. Both the data and the clock of the selected signal source are reclocked by an internal 2.5 MHz clock.

The data signal is clocked by its own clock into a 30-bit serial-in, parallel-out shift register. At the same time the signal clock operates a 5-bit counter. When a count of "30" is decoded at the output of the counter, the content of the serial counter is transferred to the 30-bit parallel buffer (Store 1). Also, if no computer readout is taking place at the time of this transfer, the 30-bit parallel word is passed on to the second buffer (Store 2). The output of Store 2 is placed, via line drivers, on the 30 parallel input lines of the 642B computer.

The decoding of the 30-bit count also initiates the computer interface protocol required for transferring the 30-bit parallel word to the 642B computer. During this transfer, the clock signal path to the Store 2 register is disabled, which prevents the contents of this register from changing. Figure 4-33 shows the salient waveforms of the CIC.

4.5.4 Computer Output Converter

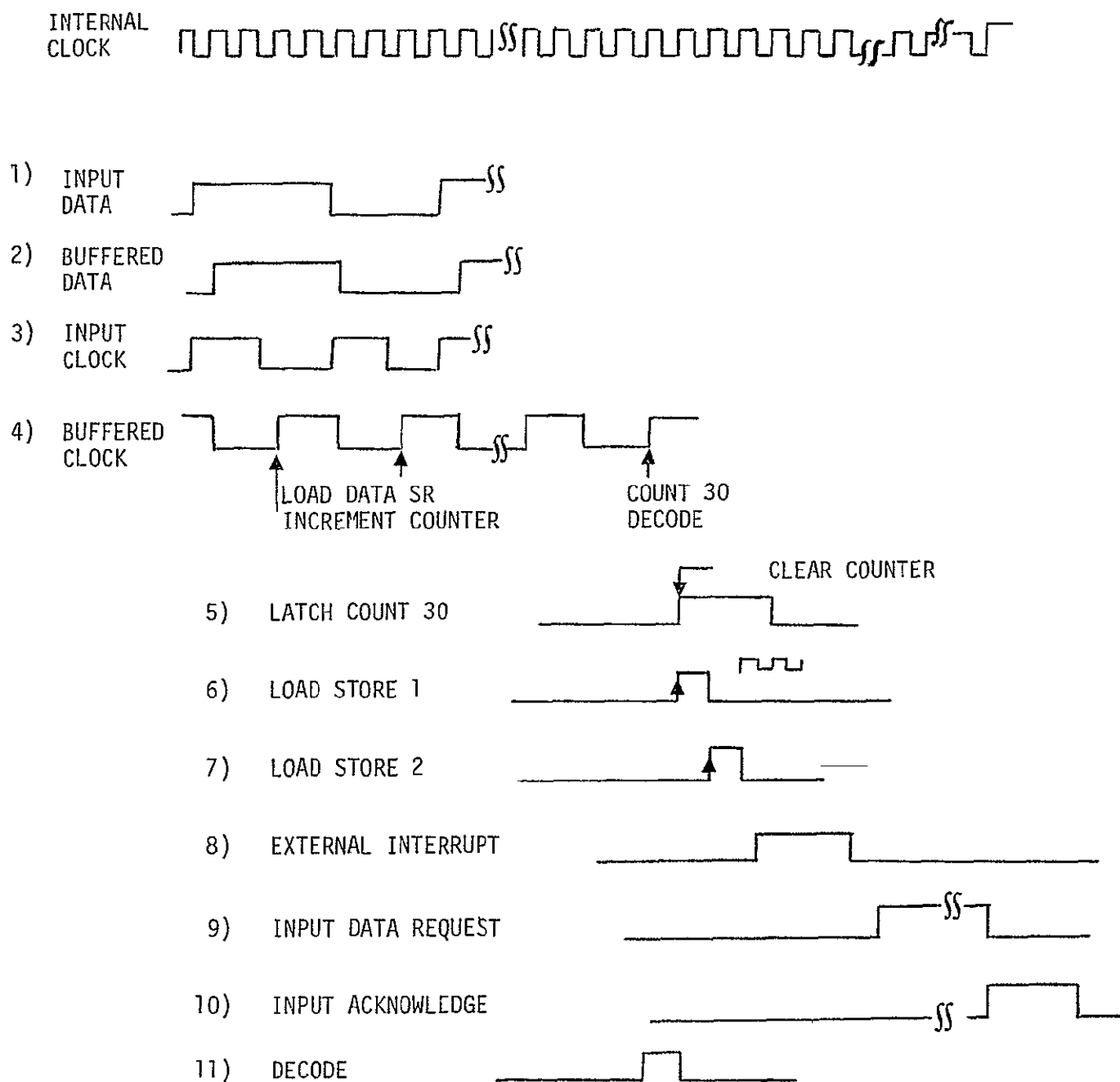
4.5.4.1 Generic Description

A generic block diagram of the COC is shown in Figure 4-34. The primary input to this equipment is the parallel data from the 642B computer. This data consists of the payload commands and configuration messages intended for the control of the PSP operation.

The main output of the COC consists of bursts of serial data transmitted to the data input terminals of either the PSP or the CIU.*

The COC serial burst data output line is bidirectional. To the PSP (or the CIU), it carries bursts of serial command data as well as bursts of the PSP configuration message data. From the PSP, it carries the PSP status message to the 642B computer. The status messages received from the PSP are converted from the serial burst format to a parallel word format. This operation is performed by the serial-to-parallel data converter.

* In this document all the discussions pertaining to the CIU burst data interface are based on an assumption that the burst interface characteristics of the CIU are similar to that of the PSP.



NOTE - WAVEFORMS 2), 3), AND 5), THROUGH 11) ARE ALL
TIMED BY THE INTERNAL CLOCK

Figure 4-33. Salient Waveforms of the Computer
Input Converter Equipment

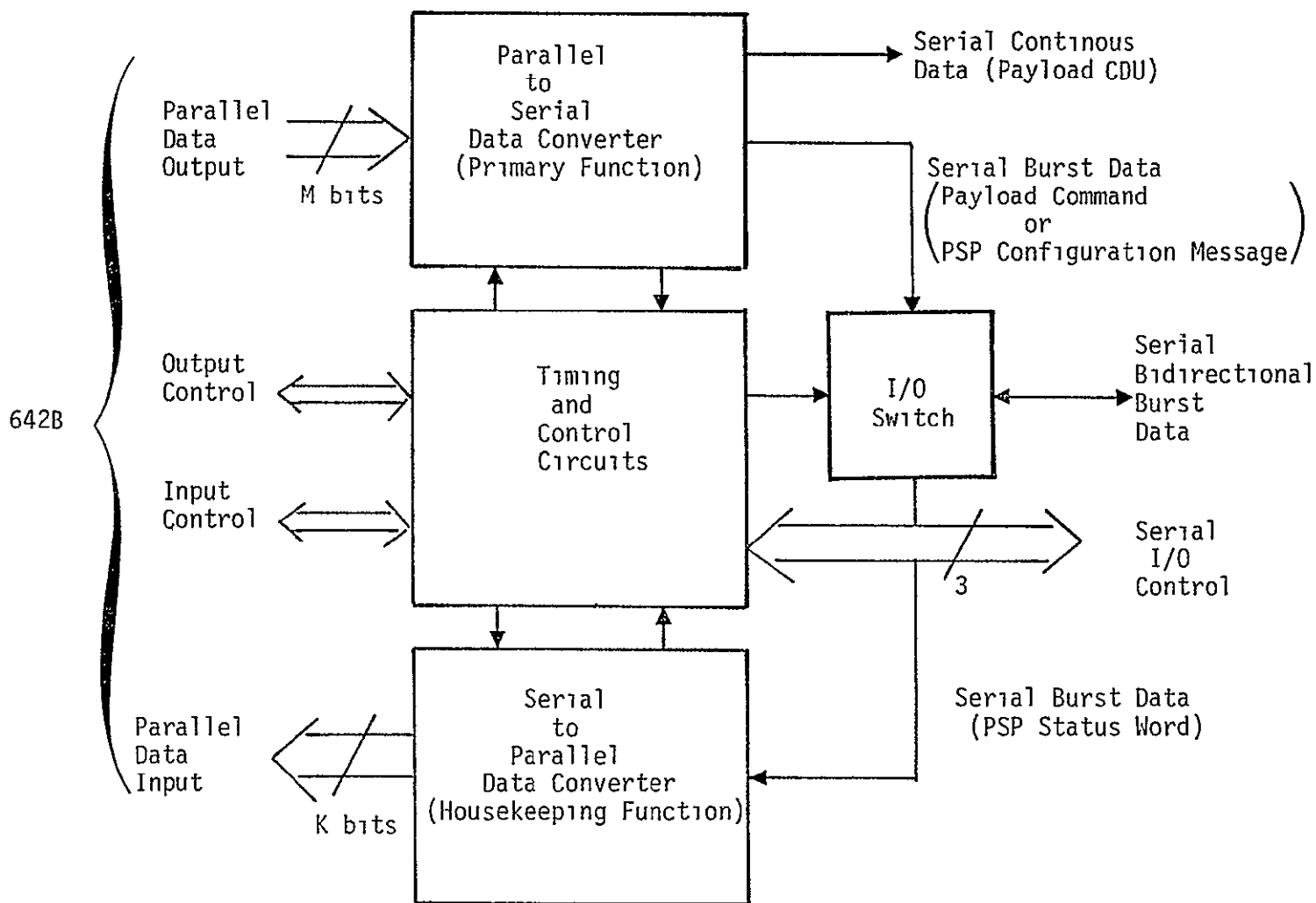


Figure 4-34 Computer Output Converter Generic Block Diagram

The passage of data to and from the COC across its three interfaces (one parallel input, one parallel output, and one serial bidirectional input/output) is determined by the protocols associated with these interfaces. The transfer of payload commands and PSP configuration messages from the 642B computer is initiated by the computer, and the transfer is performed upon the concurrence of the COC. The transfer of the status message to the COC from the PSP is initiated by the COC. The COC also initiates the transfer of the PSP status word to the 642B computer.

The Timing and Control (T/C) circuits of the COC provide all the signals required for accomplishing the appropriate conversion functions. The T/C circuits also generate all the interface control signals required to transfer the data to and from the 642B computer. In addition, the T/C circuits generate the interface control signals required to transfer data across the bidirectional interface between the COC and the PSP (or the CIU).

4.5.4.2 Functional Description

Figure 4-35 shows a functional block diagram for the COC. The major functions and their descriptions are presented in following sections.

4.5.4.2.1 Parallel Input Data Buffers

The configuration message and the payload commands are generated by the computer and delivered to the COC in a parallel format. The complete message block consists of 37 words. Each word contains 16 bits plus a parity bit. The first five words of the 37-word message are the PSP configuration words, and the remaining 32 words are the payload commands.

The configuration and command messages are transmitted to the COC on the 17 data lines at a rate of 166,667 words per second. It is the function of the parallel input data buffers to receive the 37-word message from the 642B computer and store it for subsequent read-out to the parallel data circuits. The required buffer storage consists of a 32 x 17 bit shift register stack.

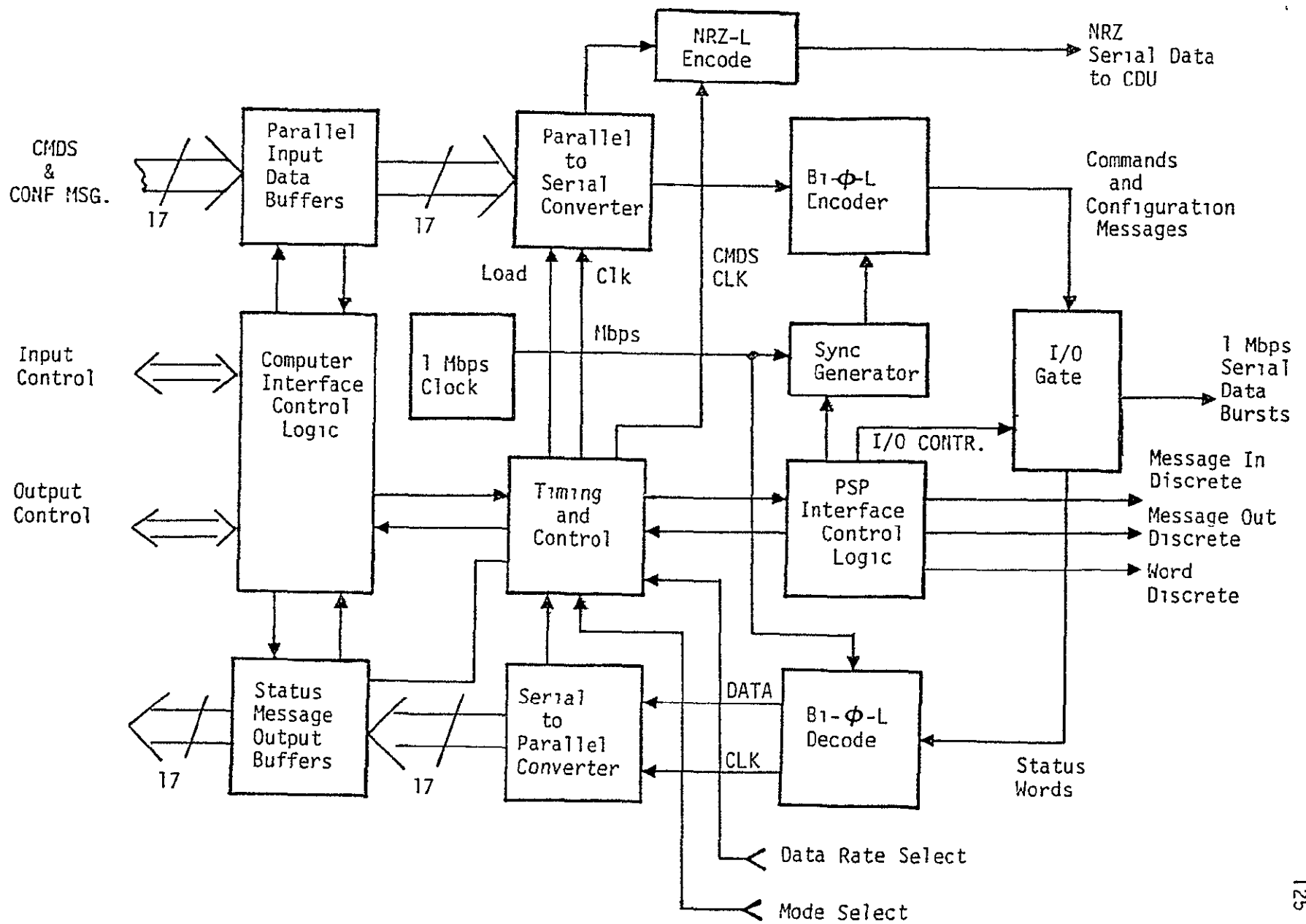


Figure 4-35. Functional Block Diagram of the Computer Output Converter

4.5.4.2.2 Parallel-To-Serial Converter

The function of this converter is to accept a 17-bit parallel word, one word at a time, and to shift this word out serially at a 1 Mbps rate when commanded to do so by the appropriate control unit. Thus, typically this converter can consist of a 17-bit, parallel in-serial out, shift register.

4.5.4.2.3 Bi- Φ -L Encoder and Sync Generator

The format for the data burst to be transmitted across the bidirectional interface to the PSP consists of 17 bits of data preceded by three synchronization bits. The three synchronization bits are a nonvalid Manchester word of 3 μ sec duration. Figure 4-36 shows the serial word format and structure. Figure 4-37 shows the data synchronization word.

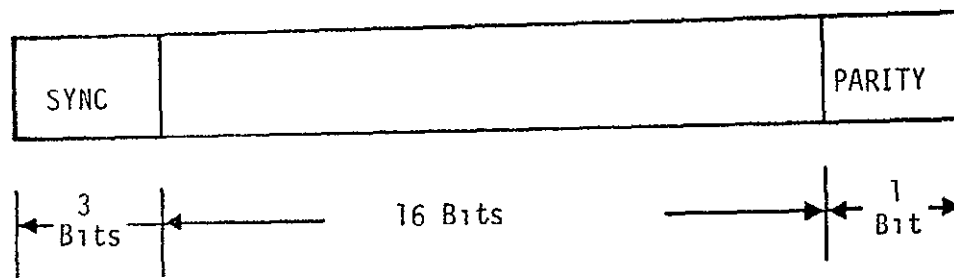
The function of the Bi- Φ -L Encoder is to add the 1 Mbs clock to the 17 bits to perform the Manchester encoding. The encoder also adds the synchronization word.

4.5.4.2.4 Input/Output (I/O) Gate

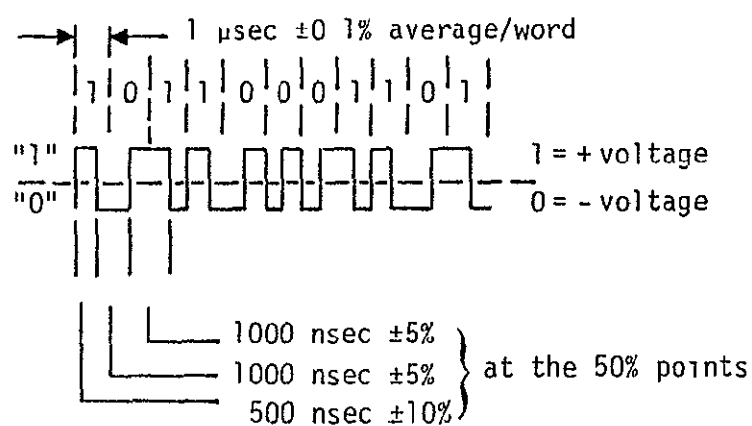
The input/output gate is a single-pole, double-throw electronic switch which is under the control of the PSP Interface Control Logic. During the "Output" mode, the switch connects the output signals of the Bi- Φ -L encoder (1 Mbps, 20-bit bursts) to the bidirectional input/output terminal of the CIC so that the configuration and the payload command messages are transmitted to the PSP (or the CIU). During the "Input" mode the switch passes the incoming 1 Mbps, 20-bit status data words to the input of the Bi- Φ -L decoder.

4.5.4.2.5 Bi- Φ -L Decoder

The function of the Bi- Φ -L decoder is to remove the 17 data bits from a 20-bit serial data burst and to transfer then 17 bits to the NRZ-L format. To accomplish this function, the decoder recognizes the data synchronization word and supplies a locally generated 1 Mbps clock of the proper phase to the decoding modulo-2 adder.



(a) Serial Word Format



NOTES B1-Phase Level (Manchester II)
 "1" represented by 10 } for Data
 "0" represented by 01 }
 "1" represented by 01 } for $\overline{\text{Data}}$
 "0" represented by 10 }

(b) Detailed Structure of the Serial Data Word

Figure 4-36. Serial Word (a) Format and (b) Detailed Structure

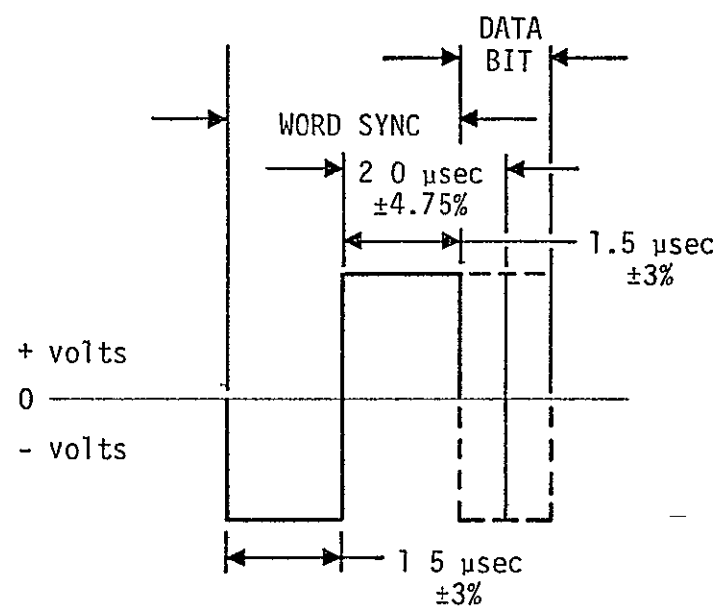


Figure 4-37. Data Word Sync, Nonvalid Manchester Code

4.5.4.2.6 Serial-To-Parallel Converter

The serial data from the output of the B1- Φ -L decoder is clocked into a 17-bit, serial in-parallel out, shift register. When the register is full, the converter signals the T/C unit to transfer the parallel word to the Status Message Output Buffers.

4.5.4.2.7 Status Message Output Buffers

The status message which is transmitted from the PSP to the computer consists of five 16-bit (plus odd parity) words. These words are stored in the 5 x 17 bit shift register stack comprising the parallel output data buffers.

4.5.4.2.8 PSP Interface Control Logic

The PSP Interface Control Logic is one of the most important subunits of COC equipment. The signals developed by this logic control the transfer of the serial burst data to and from the COC. The timing required for interfacing the COC with the PSP is shown in Figure 4-38.

As is shown in this figure, messages to the PSP can be transmitted only when the MSGOUT flag is up. Similarly, the status messages out of the PSP can be transmitted only during the time when the MSGIN flag is up. The words comprising either an incoming or an outgoing message can be transmitted over the bidirectional interface only when the corresponding WORD DISCRETE flags are up.

4.5.4.2.8 Computer Interface Control Logic

This unit controls (1) the transfer of the parallel command and configuration messages from the computer to the parallel buffers of the COC and (2) the transmission of the status messages across the parallel interface from the output buffers to the computer.

The protocol associated with this input/output transfer is given in Table 4-6 of this section.

4.5.4.2.9 Clock Oscillator

The 1 MHz clock oscillator establishes the basic timing for the internal functions of the COC equipment. It also supplies the 1 MHz carrier signal for the data burst transmission.

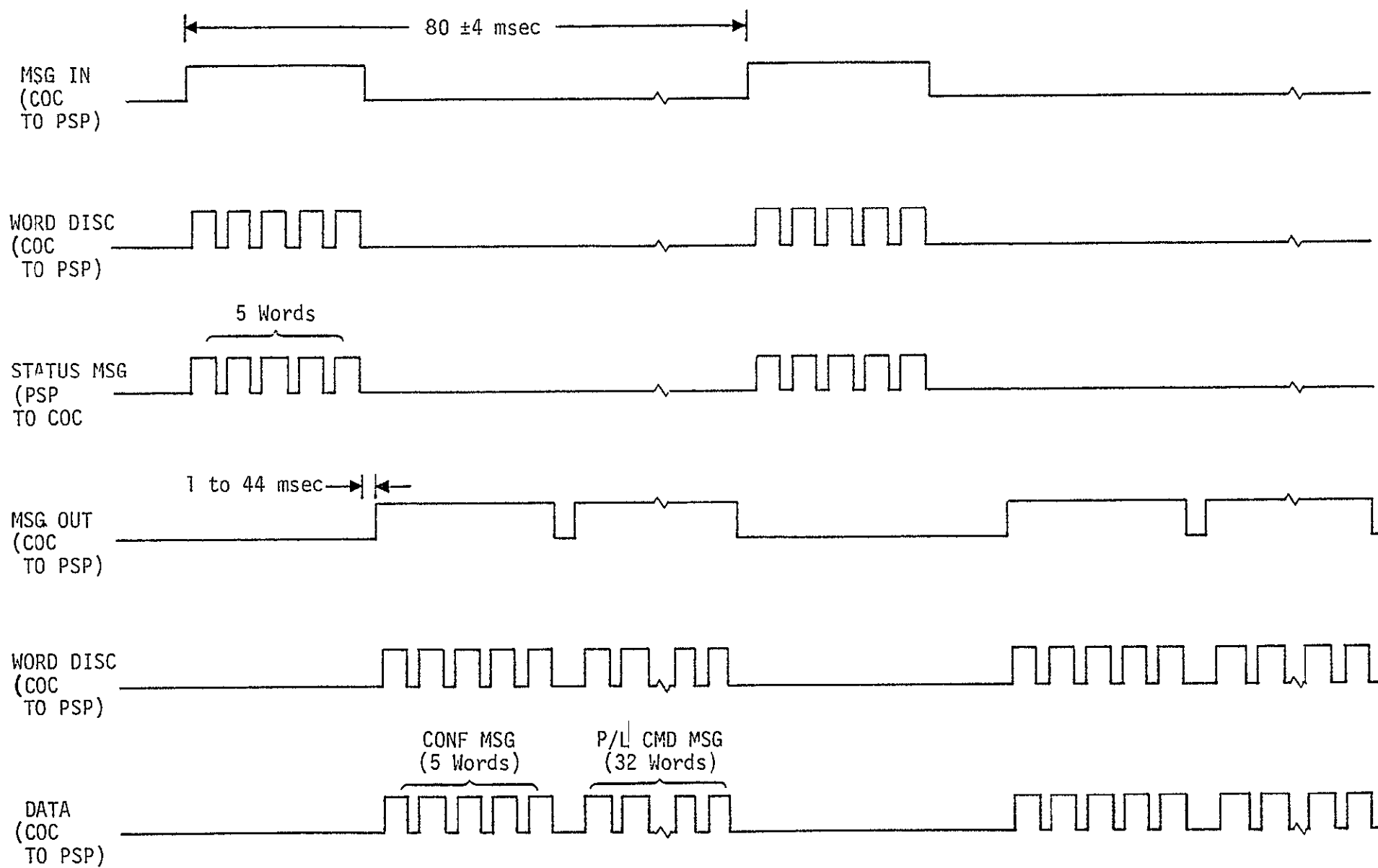


Figure 4-38. PSP Interface Timing Diagram

4.5.4 2.10 Timing and Control

The function of the timing and control circuitry is to provide the means for sequencing the transmission and reception of the data across the three interfaces of the COC. This circuitry interacts closely with the computer interface and PSP interface control logic units.

4 5.4.3 Implementation

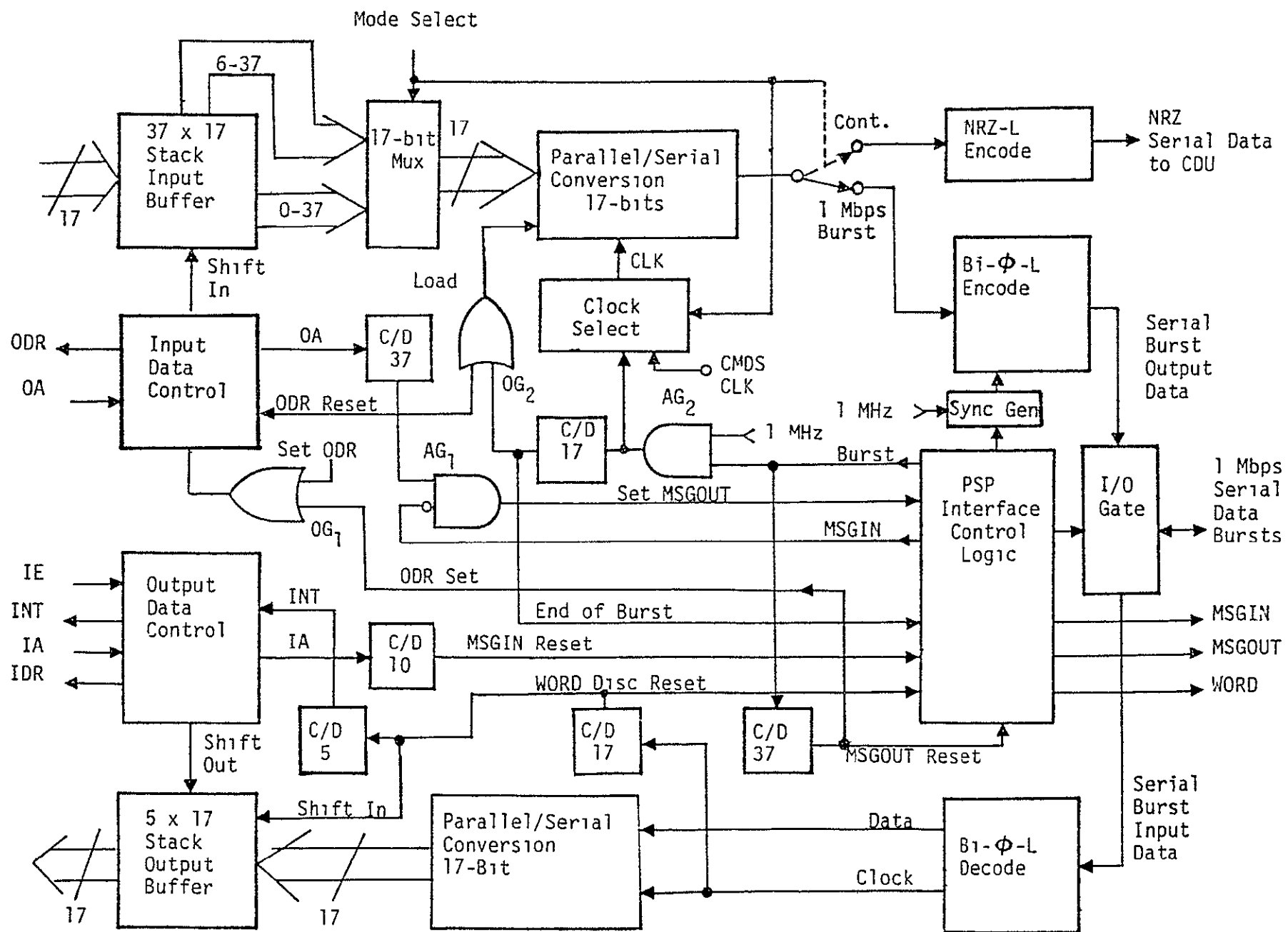
Figure 4-39 shows an implementation block diagram of the Computer Output Converter. Specifically, some of the salient components comprising the timing and control circuitry are shown.

Because the computer must examine the status word of the PSP prior to transmission of the configuration and command messages consider first the sequence in which the status word is delivered from the PSP to the computer. For this, it is assumed that the COC "wakes up" with the MSGIN raised. MSGIN signal being high makes the PSP transmit the burst commands to the COC. There are 5 words in the status message, and each message has 16 bits plus one parity bit, hence 17 bits total.

The incoming bursts are applied to the Bi- ϕ -L decoder which acts upon the sync word and outputs 17 NRZ bits to the Parallel/Serial (P/S) converter. The clocking of these bits is performed by the same clock that is used for Bi- ϕ -L to NRZ conversion. Thus, when 17-clock pulses are converted and decoded, the resultant "decode 17" pulse indicates that (1) the P/S converter shift register is full, (2) the WORD DISCRETE signal must go down, and (3) the parallel data must be shifted into the output buffer.

The process of receiving, decoding and shifting the status words is repeated until all 5 words are loaded into the output buffer. The end of the 5-word loading sequence is indicated by the "decode 5" pulse which counts the "decode 17" signals. The "decode 5" pulse is applied to the output data control unit for the purpose of initiating the External Interrupt (INT) pulse to the computer.

When the computer receives the interrupt pulse it sends to the COC an Interrupt Acknowledge Pulse (IA). Upon reception of this pulse, the COC sends to the computer the Input Data Request (IDR) pulse indicating that the COC has placed data on the input lines to the computer. The computer samples the data on its input lines and upon completion of this sampling it sends to the COC an Input Acknowledge (IA) signal.



Note C/D = Count and Decode

Figure 4-39 Implementation Block Diagram of the Computer Output Converter

This protocol is continued until all 5 words have been transferred from the Output Buffer to the computer. The end of this transfer is indicated by a "decode 10" pulse fed by the IA signals. Note that for each data word transfer there are two IA pulses. Hence, the "decode 10" is used instead of "decode 5"

Upon the completion of the status word transfer to the computer, the COC is ready to receive the configuration and command message from the computer.

The sequence of receiving the parallel data from the computer is initiated by setting the ODR line high. For this, the initialization signal is transmitted to the Input Data Control unit via gate OG₁. The input control unit then sends the ODR (Output Data Request) signal to the computer.

Having received the ODR signal the computer starts shifting the status and command words to the input buffers of the COC. The 37 words comprising the message are stored in the input buffers. The shifting of the 17-bit parallel words in the 37-word long stack is accomplished by a clock-like signal derived from the Output Acknowledge (OA) signal. This signal is generated by the computer when the data is delivered to the input of the COC.

The process of loading the status and command words continues until all 37 words have been transferred. The end of transfer is indicated by decoding 37 consecutive OA pulses.

When the decoder puts out a "decoded 37" signal, this signal performs three functions: (1) it resets the ODR line to "low," (2) it loads the first word into the parallel input of the P/S converter, and (3) it enables one of the inputs of the MSGOUT gate AG₁. If the MSGIN signal is low, indicating that no messages are being received from the PSP, the "decoded 37" signal is passed through AG₁ and appears as a Set MSGOUT signal at the input to the PSP.

At the same time, the PSP control logic initiates the sync generator, placing the data word sync pulse on the input of the B1- Φ -L encoder. Following this event, a burst pulse is applied to gate AG₂. This pulse admits the 1 MHz clock to the P/S converter, and the contents of the converter are read out serially.

The end of the readout is indicated by a "decode 17" pulse which is fed by the 1 MHz clock admitted to the P/S converter. The

appearance of the "decode 17" pulse then (1) signals the "end of burst" to the PSP logic control and (2) reloads the P/S converter for the next burst. This transfer is continued until all 37 words have been transferred to the PSP. The end of the transfer is indicated by a "decode 37" pulse which is developed by a counter fed by the burst commands emerging from the PSP control logic.

The "decode 37" also sets the ODR line, thus making the COC input circuits ready for reception of another 37-word message from the computer. It also applies the MSGOUT Reset signal to the PSP control logic.

When operating in the serial and continuous commands output mode, the loading of the input buffer is performed in a conventional manner (i.e., all 37 message words are admitted). However, for readout only, words 6 through 37 are applied to the P/S converter. The rate of the serial readout for this case is controlled by an appropriate command clock. Also, the rate of command input to the COC from the computer is adjusted accordingly to provide continuous flow of serial data output.

5.0 ESTL INTEGRATION AND SIMULATOR CHECKOUT

5.1 Physical Characteristics

The payload simulator equipment can be logically subdivided into two categories: (1) the payload simulator, per se, and (2) the 642B computer interface equipment. These equipments are comprised of various subunits as follows

1. Payload Simulator (upright cabinet rack)
 - (a) Receiver
 - (b) Transmitter
 - (c) Frequency synthesizer
 - (d) Command detector unit
 - (e) Telemetry modulator
 - (f) Power supplies
2. 642B Interface Equipment (two separate cabinets)
 - (a) Computer Input Converter (serial/parallel)
 - (b) Computer Output Converter (parallel/serial)

Each of the subunits forming the payload simulator is envisioned as a slide-mounted drawer which fits into the main cabinet rack. The slide mounting of the racks will provide for easy access to the inside of the drawers for the purpose of maintenance and service. The location of the simulator rack will be inside Shielded Enclosure #3 (SEN 3) of the ESTL facility

The interface equipment will be enclosed in two separate cabinets. The computer Input Converter (CIC) will be in one cabinet and the Computer Output Converter (COC) will be located in a second cabinet. Both interfaces will be mounted into the Video Support/Digital Equipment rack group located in the Test Control Center area (Room 121). Such mounting will minimize the length of the multiwire cables (MWC) required to establish the parallel wire connections between the interface units and the 642B computer located within the Data Processing Area.

The physical dimensions of the subunits comprising the payload simulator equipment are shown in Figure 5-1. The dimensions indicated are approximations to the nearest inch of the standard dimensions for the enclosures. The front panels of all units, regardless of enclosure size, are standard 19-inch panels.

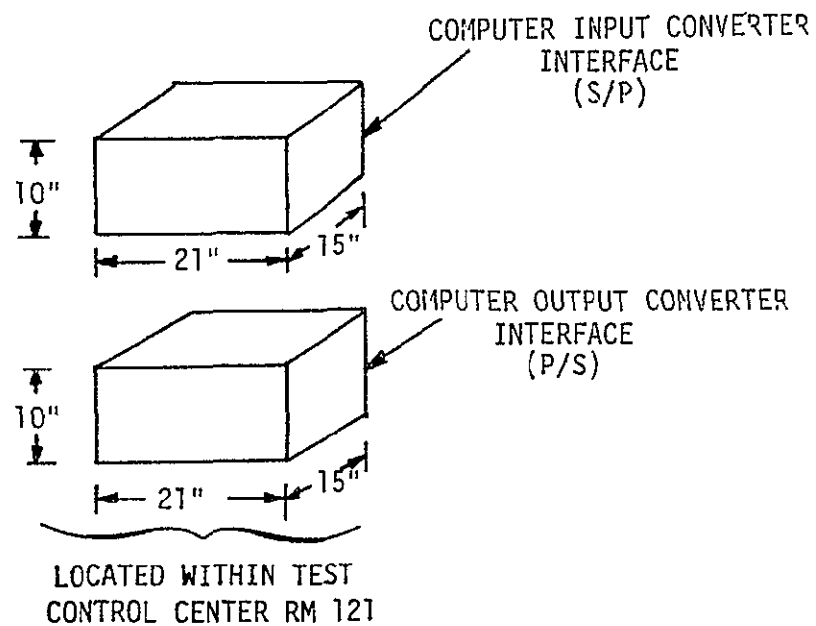
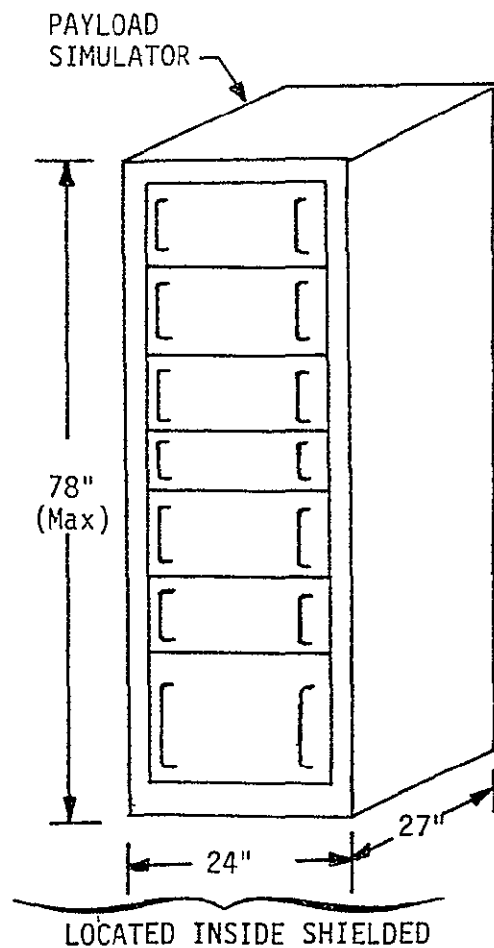


Figure 5-1. Physical Dimensions of the IUS/Payload Simulator Equipment Group

As can be seen from Figure 5-1, the major component of the simulator equipment group is the payload simulator upright cabinet rack. Because this rack has to fit into the shielded enclosure (whose inside dimensions are 20 feet wide, 10 feet deep, and 7 feet 4 inches high), the maximum height of the rack is limited to about 6.5 feet (i.e., 78 inches).

In comparison, there is no specific limitation on the sizes of the subunits located outside the shielded enclosure and their dimensions are thus dictated primarily by their contents.

5.2 Environmental

The simulator test equipment will be operated indoors, within the confines of the ESTL. This implies a laboratory environment characterized by a temperature range from +50°F to +100°F (+10°C to +38°C).

The temperature environment permits the use of digital ICs specified for the 0°C to 70°C temperature range. For TTL logic ICs, this permits the use of the relatively inexpensive and readily available 7400 family, or an equivalent.

The specification for the simulator does not require any one component to generate (and therefore dissipate) a considerable amount of power. Furthermore, the rack space available is adequate and also provides for good distribution of components commensurate with low interference level requirements. Consequently, heat dissipation is not considered a severe problem. Forced air cooling will be provided for the cabinet to insure that no heat pockets are formed within the card cages and RF equipment drawers. Air flow will be via RF shields to maximize interference rejection, specifically within the receiver drawer.

5.3 Electrical and Grounding

The primary power source for the simulator equipment will be a 115 VAC $\pm 10\%$, 60 Hz single-phase line. Each cabinet will have its own power supply for developing the required operating DC voltages. The AC line input to the power supply of each cabinet will contain a circuit breaker of suitable rating to protect the equipment.

Within the main cabinet rack, the power supply implementation can proceed along the following two approaches:

- (1) Use of a single AC input to a power supply drawer where all the required DC voltages are generated and distributed to respective drawers.
- (2) Distribution of the AC to the individual drawers where the power supplies develop the voltages required for that particular drawer.

With the first approach, the RFI suppression is easier because power supply inputs to the drawers are at relatively low voltages. Thus, RFI filters do not have to be as expensive as those required for the power line AC filtering.

Adequate grounding will be provided by connecting each drawer to the grounding bar of the rack by a conductive braid. The grounding bar will be connected to the ground terminal of the shielded enclosure

5.4 Signal Routing and Interfaces

Figure 5-2 shows the signal routing and interfaces between the IUS/Payload simulator and the various functional areas of the ESTL. As shown in the figure, the main cabinet rack of the simulator is located inside SEN 3 of the ESTL. The cables which interface with the equipment located at other areas are of two types, RF cables and baseband information cables. The RF cables interface only via the Space Loss Simulator and the RF Path Console, the latter located within SEN 1.

The important feature of the RF interconnection to be used with the payload simulator is that two separate cables (RG-214) are employed. One cable carries the PI signal to the PS receiver; the second cable carries PS output transmissions to the PI receiver. The main reason for providing such separate interfaces is to allow independent controls (attenuators) for the forward and return links to the payload. With this arrangement, threshold performance of either the PI or the PS can be determined separately. Furthermore, the effect of the space loss on both units can be tested by "ganging" the action of the two RF attenuators within the space loss simulators.

In addition to the variable attenuators, which can provide up to 120 dB attenuation each, the "fixed" path loss between the payload and the PI units is estimated at about 76 dB. This fixed path loss is comprised of about 44 dB RF path console loss and close to 32 dB of RF

cable loss. The total fixed loss of 76 dB is approximately the same for both the PI-to-PS and the PS-to-PI links.

The baseband signal cables interface the inputs and outputs of the IUS/Payload simulator with Shuttle avionics equipments such as the PSP and the CIU. The baseband cables also interconnect the PS equipment rack with the interface equipments. Furthermore, as is shown in Figure 5-2, several interconnecting cables are required between the PSP and the 642B interface equipments.

The likely candidates for most of the baseband signal interconnections are the single-ended, 50-ohm coaxial cables. The ESTL has a considerable number of such cables already installed for interconnecting various areas of its facility. A convenient use of such existing cables can thus be realized. Furthermore, if additional cables are required to accommodate the payload simulator function, such cables can be provided by the ESTL.

The six cables (13 through 18) which interconnect the PSP and the 642B interface units require special consideration because, as shown in Figure 5-2, they may have to be twin-lead cables (TLC), differentially driven, to be compatible with the PSP input/output (I/O) interfaces [2]. Such cables are not generally used for ESTL area connections, but they may be provided if absolutely necessary.

An alternate approach would be to provide a set of twin-lead cable/single-lead cable converters in proximity to the PSP unit, as well as other avionics units using such twin-lead cables. The single-ended, coaxial outputs of such TLC/SLC interfaces can then be handled in a conventional manner by the ESTL signal distribution function. One of the desirable features of the simple single-ended cables is that they can easily interface with the patch panel, thus increasing the flexibility of the test setup.

It must also be noted that, as shown in Figure 5-2, cables 15 through 18 must be connectable to either the PSP or the CIU. These four cables are used for transferring commands in a burst format from a command source (a parallel-to-serial interface in our case) to the PSP. In Shuttle avionics equipment terminology, such an interface is called a Multiplexer-Demultiplexer (MDM) interface. Because one of several command inputs to the CIU is accepting commands via an MDM interface, the

payload simulator setup must also provide such a capability.

The connections to the CIU shown as dotted lines in Figure 5-2 indicate that cables 15 through 18 can be simply transferred from the PSP connectors to an equivalent set of connectors on the CIU.

An alternate approach would be to provide a patch panel capable of performing this function. This patch panel could be a part of the ESTL in-house equipment.

Another interface function which requires special consideration is that of providing proper interconnecting cables for DOD encryptor and decryptor units. The encryptor unit is used, when required, to encode the outgoing telemetry data stream. Similarly, a decryptor must be used to decode the commands being sent to the PS unit from the CIU.

As indicated in Figure 5-2, the major difference between the cabling requirements for the encryptor and the decryptor is the number of wires needed for each of these interfaces. Specifically, the telemetry encryption can be handled by a single-ended coaxial cable, while the command decryption requires 4-wire input/output cabling.* These factors will have to be taken into consideration when determining the location of the encryption and decryption equipment within the confines of the ESTL.

A means for testing the performance of the NASA command detection unit (CDU) with the PS is provided in the cabling setup shown by two video noise summers placed in lines 10 and 19. Line 19 supplies the baseband NRZ-L commands from the P/S interface units directly to the bit sync subunit of the NASA CDU. Adding a controlled amount of video noise to this baseband signal will provide for calibration of the bit detector performance.

A similar test involving the command data modulated on the 16 kHz subcarrier can be performed by insertion of a video noise mixer into line 10 to the PS input. This test permits the evaluation of both the subcarrier demodulator and the bit synchronizer. By measuring the difference in the performances of the two units, the degradation due to the subcarrier demodulation process can be determined. The two noise summers discussed above are shown in Figure 5-2. These units will be provided by the ESTL, similar to the space loss simulators.

* Four separate wires are required to handle independently the "S," "0," "1," and CLK signals.

Other interface equipment to be provided by the ESTL are the multi-wire (90-wire) cables used for connecting the S/P and the P/S interfaces to the 642B computer.

5.5 Test Equipment Requirements

The payload simulator group is essentially a piece of special-purpose test equipment, and it should be so designed that it requires a minimum of built-in test equipment. The test equipment usage philosophy for the simulator is that it should not require built-in (captive) equipment which can be readily obtained from the ESTL calibration lab. Thus, such expensive equipments as general-purpose spectrum analyzers and noise figure test meters should not be incorporated into the simulator enclosures. However, test points and terminals will be incorporated into the simulator equipment to provide for ease of test equipment use when required.

As a minimum, the following test equipment will be required to test and check out the simulator equipment:

1. Spectrum analyzer (HP Model 8555 with 8552B IF section and 141T mainframe display, or an equivalent equipment)
2. Noise figure meter (HP Model 949A, or equivalent)
3. Frequency counter (HP Model 5245L with 5254C heterodyne converter, or equivalent)
4. High frequency oscilloscope
5. Digital multimeter
6. Low frequency (<2 MHz) function generator

These equipments are general enough to be considered as potentially available GFE from the ESTL. Thus, they do not represent any unusual, hard-to-meet requirements. Special equipment requirements are outlined in Section 5.6 and Appendix C.

5.6 Acceptance Tests

5.6.1 General Test Summary

The simulator equipment will undergo acceptance testing at the JSC and the results of these tests will be documented to indicate compliance with the PS equipment specifications.

The purpose of these tests will be twofold: (1) to verify that equipment performance is within acceptable limits at the installation site and (2) to familiarize the ESTL personnel with the functioning of the simulator equipment. The nature of calibration and operational tests is defined in Section 3.3 of this report; Table 3-1 lists those specific tests that should be conducted.

Section 5.5 indicates the basic test equipment required to perform calibration and operational tests. For some tests, additional equipment is needed. Other measurements necessitate special hardware configurations. And lastly, a few tests can be successfully conducted only through the use of the sampled-data techniques outlined in Appendix C.

Table 5-1 lists the PS acceptance tests in the general order in which they should be performed. The tests listed in Table 5-1 are only those to be conducted on the delivered PS equipment for acceptance purposes. Also indicated is the primary (Task 501-oriented—see Section 3.0) or secondary nature of the test, whether additional equipment beyond that specified in Section 5.5 is required, the need for additional hardware or special configurations, and whether sampled data instrumentation (Appendix C) is recommended.

5.6.2 Some Test Commentary/Notes

5.6.2.1 Noise Figure Measurement

The result of this test is dependent on the receiver operating frequency; therefore, the receiver programmable frequency synthesizer should be set to the proper value corresponding to the desired receive frequency. It is also recommended that the measurement be made with the tracking loop in the "open" position. A calibrated noise source with a noise figure on the order of that of the receiver should be employed for highest accuracy. A sampled-data measurement approach in lieu of a noise figure meter is discussed in Appendix C.

5.6.2.2 PLL Natural Frequencies

A knowledge of the BPL suppression factor at the PLL operating design point is needed. It may be determined through calculation based upon the noise bandwidth of the crystal filter(s) and the operating point receiver input signal-to-noise spectral density ratio [4].

Table 5-1. PS Acceptance Tests

Subsystem	Test	Nature		Additional Test Equipment	Additional Hardware/ Configuration	Sampled-Data Techniques
		Primary	Secondary			
All	Power Supply Voltages and Currents	X				
Receiver	Gain From Input to Power Monitor Port	X				
	Noise Figure Measurement	X				X
	VVA Characteristic	X				
	Gain From VVA to 10 MHz IF Hybrid	X				
Receiver	Spurious IF Spectra		X			
Receiver	Crystal BPF Noise Bandwidths	X				
	IF Limiter Output		X			
	PLL Natural Frequencies	X		X		
	Input Frequency Tuning		X			
Receiver	Demodulated Command Waveform Check	X				
	Demodulated Ranging Waveform Check	X				
Receiver	Strong Signal Phase Noise	X				
	Phase Detector Noise Biasing		X			X
Receiver	AGC Versus Signal Level	X				X
	Absolute Threshold		X	X	X	X
	Minimum Operating Conditions	X				X
	Swept Frequency Acquisition		X			
	Lock Detector Statistics	X				X
Receiver	Command Waveform SNR		X			X
	Ranging Waveform SNR		X			X

Table 5-1 (contd)

Subsystem	Test	Nature		Additional Test Equipment	Additional Hardware/ Configuration	Sampled-Data Techniques
		Primary	Secondary			
Receiver	Ranging Relative Phase Shift		X	X		
	Ranging Signal Delay	X		X		
Transmitter	Phase Modulator Deviation	X		X	X	X
	Linearity					
	Phase Modulator Frequency Response	X		X	X	X
	Forward Link Modulation Feedthrough	X			X	
	Phase Modulator Intermodulation Levels		X	X	X	
	Output Composite Spectra		X			
	Amplitude Modulation Components		X		X	
Transmitter	Output Power Levels	X		X		
	Output VSWR		X	X		
	Output Impedance		X	X		
Telemetry Modulator	PSK Output Waveform	X		X		
	FM Frequency Response		X	X		
	FM Deviation Sensitivity		X	X		
	FM Output	X		X		
Command Detector	AGC Control Range	X		X		
	NRZ Detector/Synchronizer Performance		X	X		X
	SGLS Symbol Error Rate	X		X		
	NASA Bit Error Rate	X		X		
	Lock/Squelch Statistics	X		X		X

The most accurate means of measuring the PLL operating point natural frequency is to reduce the signal level output of the limiter by an amount equal to the operating point suppression factor (a 50 Ω variable attenuator inserted into the circuit will suffice) and measure the tracking loop phase detector output when a FM test transmitter (connected to the receiver input) is being frequency modulated by a low frequency sinusoid. The frequency of the sinusoid for which maximum dynamic phase error is obtained is equal to the PLL natural frequency.

The natural frequency determination may also be made without attenuating the limiter output signal, however, the measured natural frequency obtained must then be converted to the operating point natural frequency through calculations. This approach is usually less accurate than that of attenuating the limited output because the PLL operates in a highly damped condition

5.6.2.3 Phase Detector Noise Biasing

See the discussion in Appendix C.

5.6.2.4 Absolute Threshold

This measurement should be made with no carrier modulation and with as little frequency detuning or loop stress as possible. The SNR in the PLL noise bandwidth is set to 0 dB and the loop RMS phase error is measured

5.6.2.5 Carrier SNR

See Appendix C.

5.6.2.6 Ranging Relative Phase Shift

This measurement is with respect to the STDN tone ranging signal. Specific procedures may be obtained from GSFC documents.

5.6.2.7 Transmitter Phase Modulator Measurements

See the additional hardware/configuration discussion in Appendix C.

5.6.2.8 Command Detector Performance

Appendix C outlines a signal-to-noise ratio estimation technique.

5.7 Simulator Environmental, Operating, and Documentation End Item Criteria

The PS, when delivered and installed in the ESTL, must satisfy various environmental, operating, and documentation criteria. The more important of these criteria are tabulated in Table 5-2.

Table 5-2. End Item Criteria

Operating Temperature Range	+50°F to 100°F (+10°C to 38°C)
Power Source	115 volts AC $\pm 10\%$, 60 Hz single-phase
Structural	Capable of withstanding cross-country ground transportation
Mechanical	Standardized construction techniques Standardized front panels (19-inch rack compatible) Standardized interface connections*
Safety Guidelines	Protection of test operator during use and maintenance Circuit breakers of suitable rating to protect equipment
Drawing	Commercial grade manual
Quality Control	Best commercial practices
Operational and Maintenance	Commercial-grade manual (theory, schematics, and key waveforms) Highly skilled technician Periodic calibration will be a standard procedure

* 642B requires special interface connector

• 6.0 COST PROJECTIONS

See separate Cost Volume

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7.0 PAYLOAD SIMULATOR PHYSICAL PANEL CONFIGURATIONS AND OPERATING FEATURES

Previous sections of this report have discussed the detailed PS hardware design (Section 4.0) and certain of its characteristics necessary for conducting system tests (Sections 3.0 and 5.6). The "Specifications for IUS/Payload Communication System Simulator Equipment" (Appendix A) states specific operational features and conveniences for the physical equipment, especially in terms of the mode and option selection, indicators, controls/switches, meters, and test points.

In order to provide the reader with a detailed physical orientation to the PS, conceptual drawings of the rack panels which comprise all of the major subsystem units have been provided. These are pictured in Figures 7-1 through 7-9. For the most part, they are self-explanatory. Details of the features may be found in Section 4.0 and in the Specification (Appendix A).

It should be noted from these figures that normal or operational signal input and output connectors are not located on the front panels. Rather, they are made available at the rear of each subsystem assembly, where cables are connected and routed to the rear of the rack cabinet and out through an opening in the rack baseplate

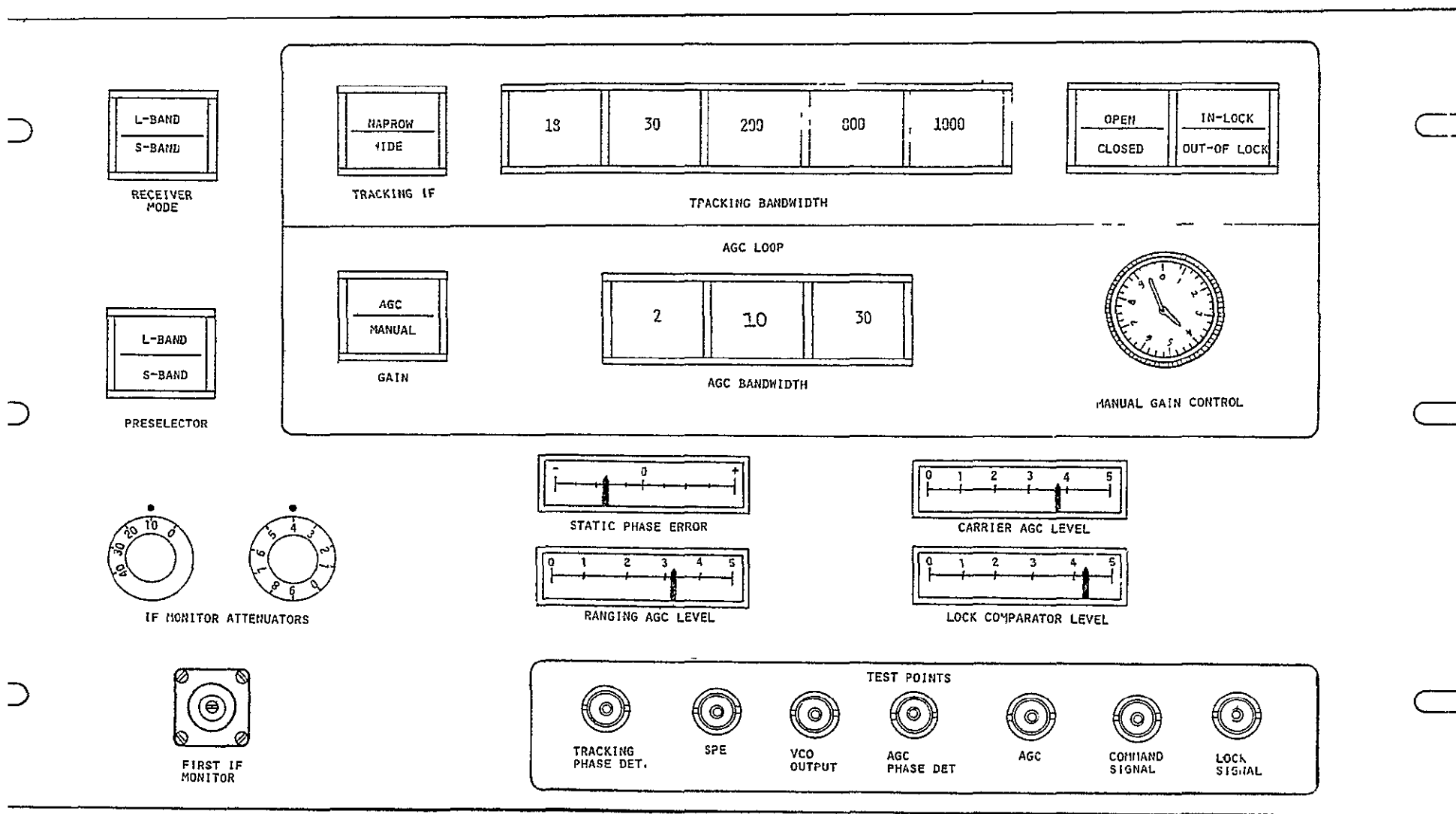


Figure 7-1. Receiver Panel

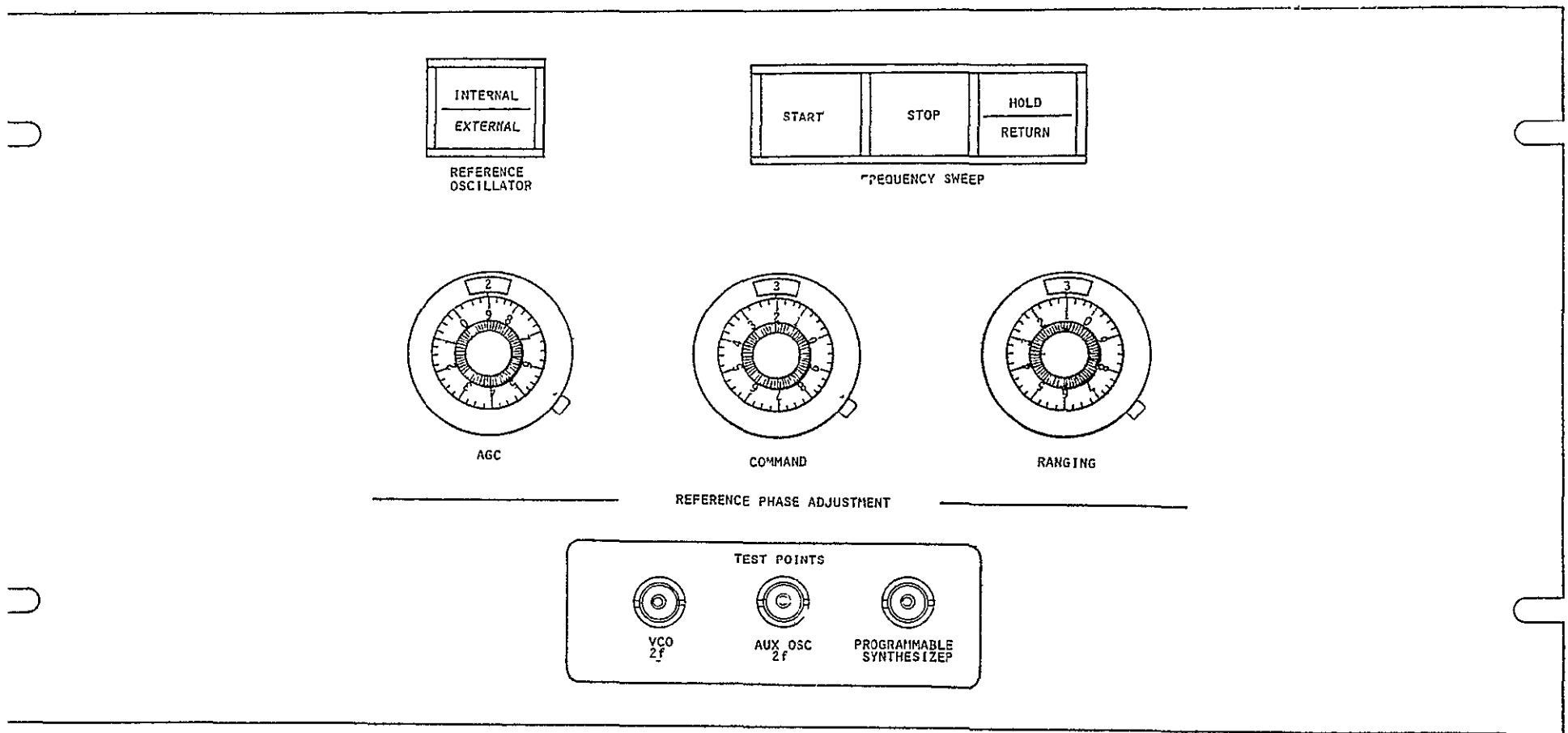


Figure 7-2. Frequency Synthesizer Panel

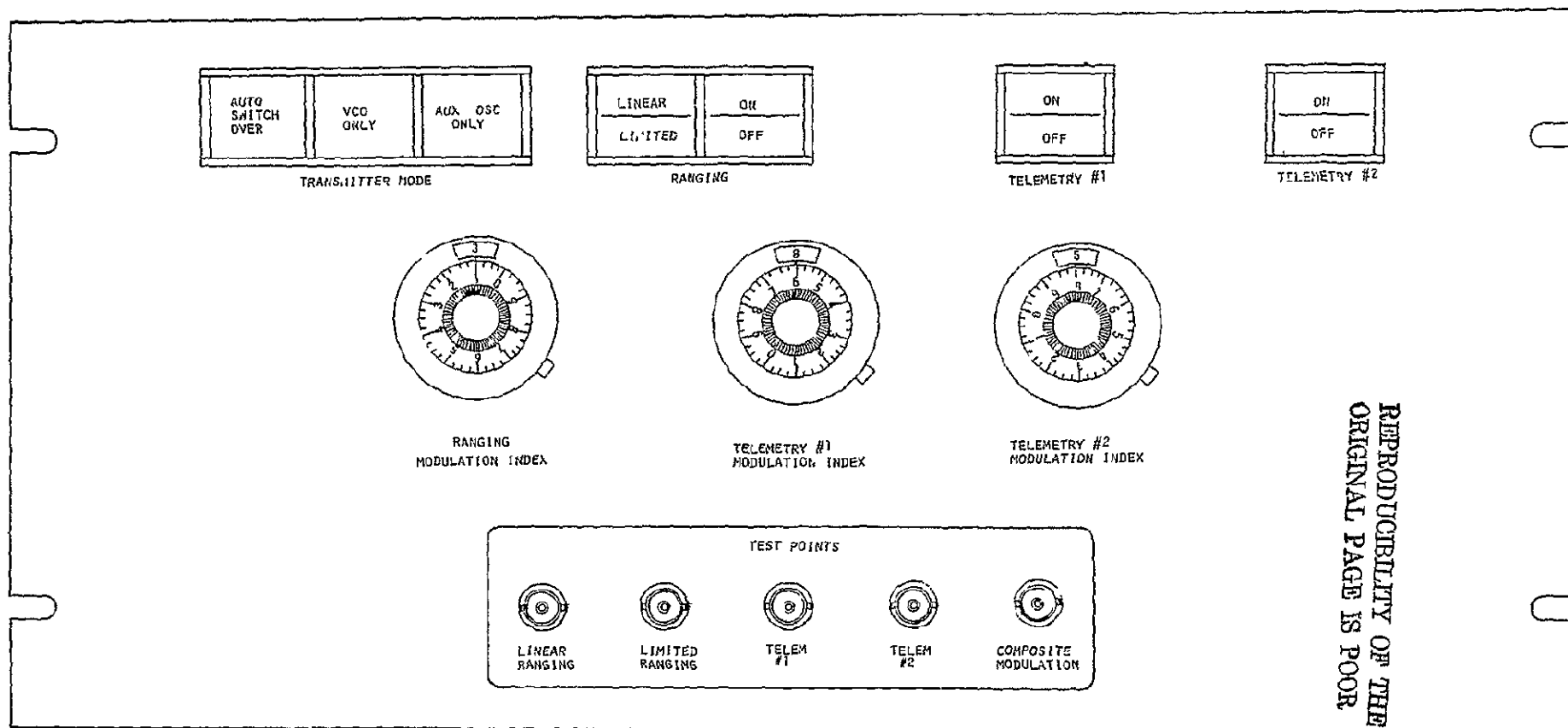
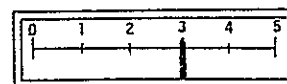
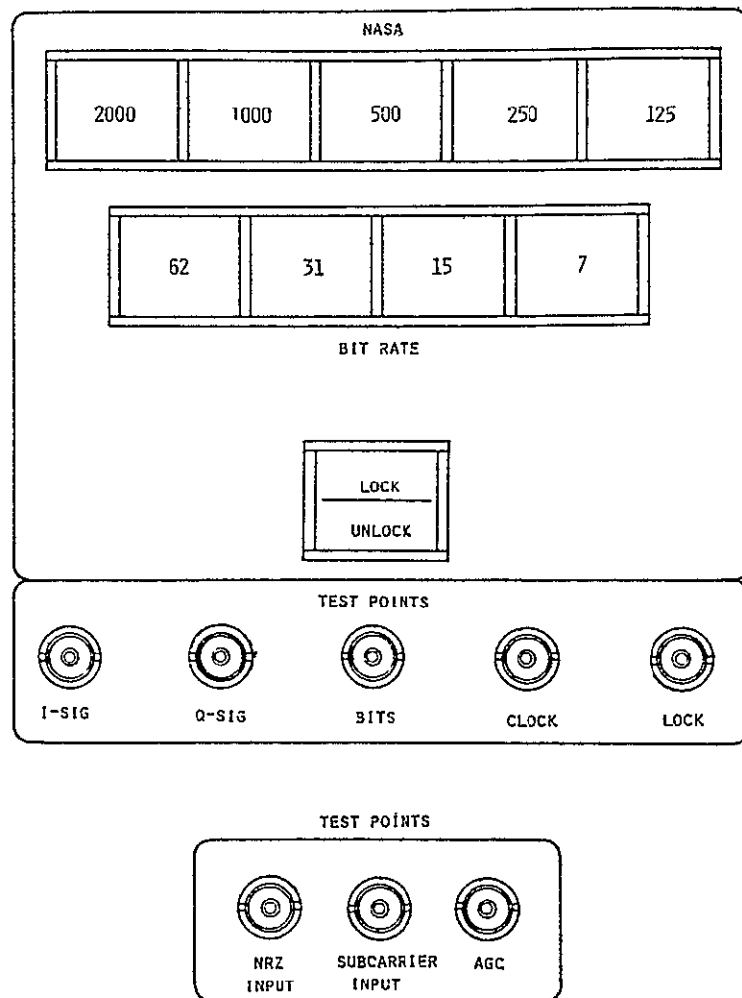
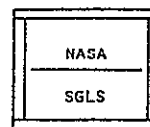


Figure 7-3. Transmitter Panel

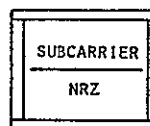
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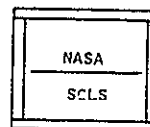
AGC LEVEL



MODE



INPUT



SELECTED
OUTPUTS

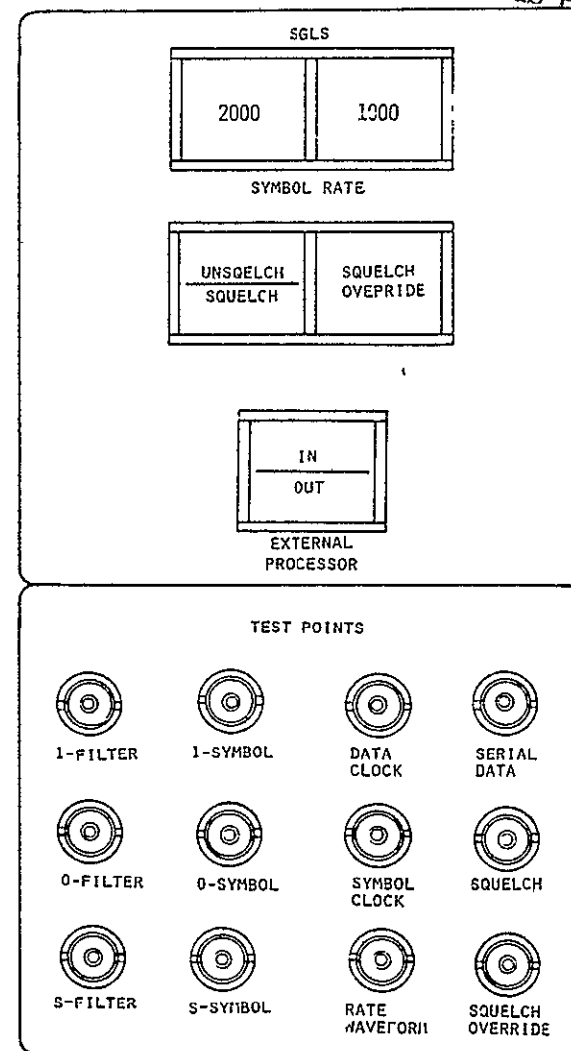
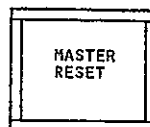


Figure 7-4. Command Detector Panel

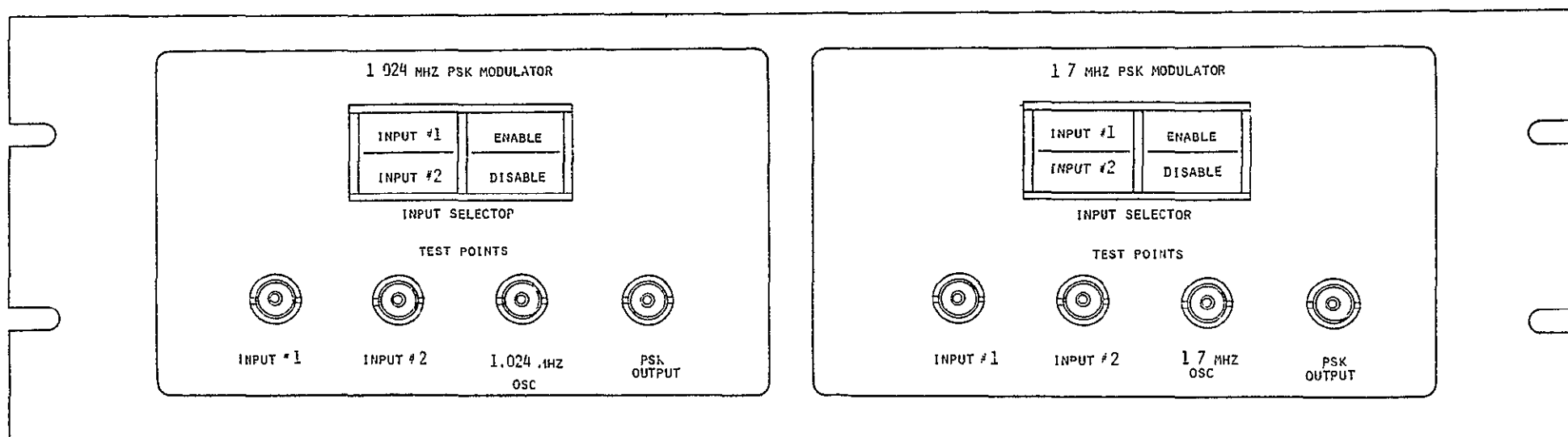


Figure 7-5 PSK Modulator Panel

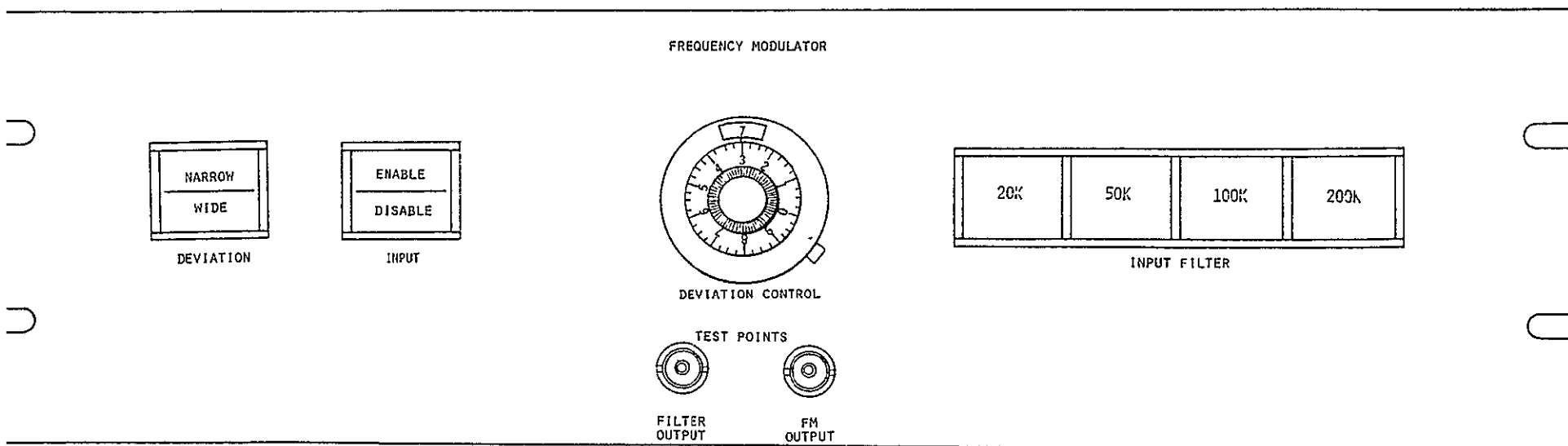


Figure 7-6. Frequency Modulator Panel

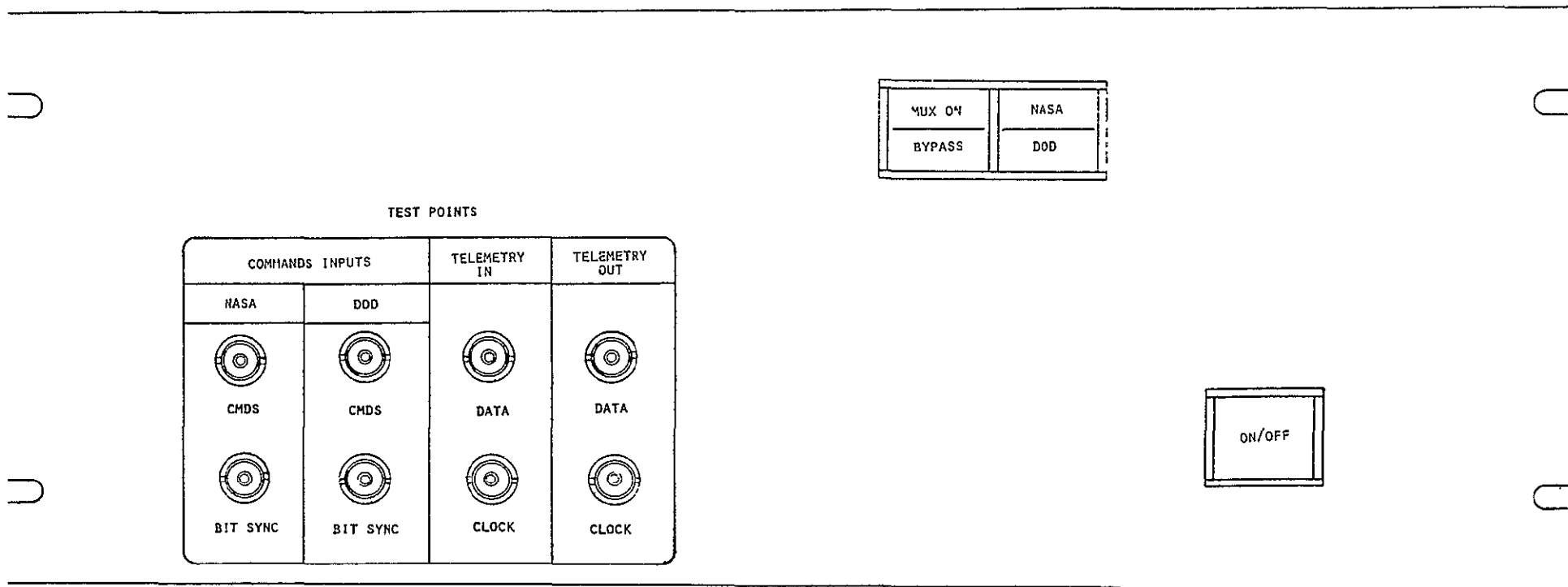


Figure 7-7. Multiplexer Panel

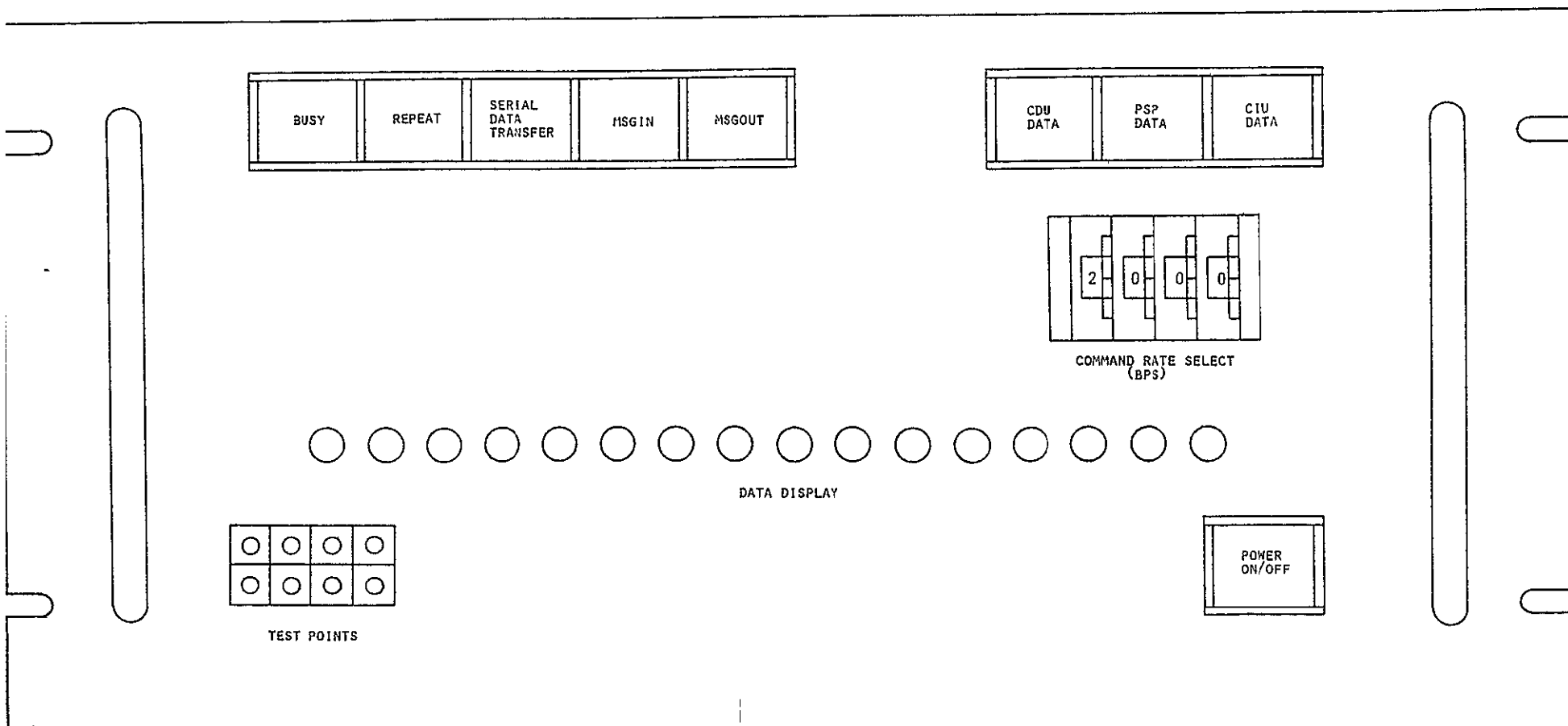


Figure 7-8. Computer Output Converter

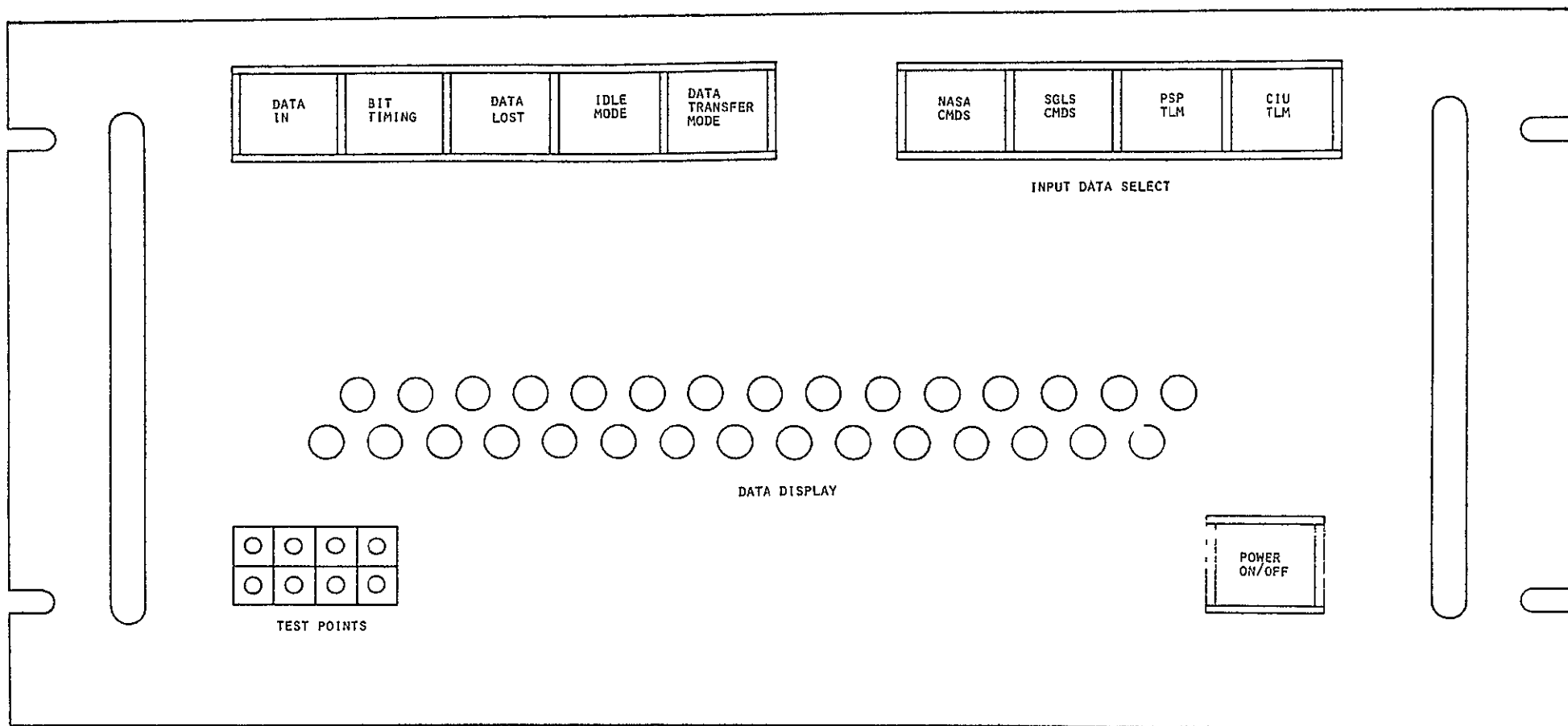


Figure 7-9. Computer Input Converter

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APPENDIX A

SPECIFICATIONS FOR IUS/PAYLOAD COMMUNICATION SYSTEM SIMULATOR EQUIPMENT

APPENDIX A

SPECIFICATIONS FOR IUS/PAYLOAD COMMUNICATION
SYSTEM SIMULATOR EQUIPMENT

The specifications are included in a separate bound document,
Report No. R7801-5.

APPENDIX B
COST DETAILS

See separate Cost Volume.

APPENDIX C

SAMPLED DATA MEASUREMENTS AND MONITORING

APPENDIX C

SAMPLED DATA MEASUREMENTS AND MONITORING

1 0 INTRODUCTION

Sampled data measurement techniques may be judiciously applied to the Payload Simulator as a means of calibrating and monitoring key performance parameters. Using a minicomputer or microprocessor, highly accurate complex determinations may be obtained for a low to moderate cost, obviating the need for highly specialized test equipment which serves only limited functions. The flexibility effected through simple stored program changes makes one general set of digital hardware amenable to essentially any measurement.

Some of the measurements that may be undertaken via the sampled data approach are listed in Table 1. Many of these are outlined in the following sections of this appendix. Detailed explanations and implementations are beyond the scope of the present text, however, Axiomatic will further study and develop any or all of these measurement techniques for JSC, if such proves desirable.

2 0 BASIC SAMPLED DATA MEASUREMENT CONCEPTS

In this section, an elementary phase detector type receiver is developed, and sampled data algorithms are applied to illustrate the concepts involved.

Figure 1 shows a model of the system under discussion. The signal $S(t)$ will be defined as a phase modulated carrier according to the following equation.

$$S(t) = \sqrt{2P_T} \cos [\omega_0 t + \theta m(t)], \quad (1)$$

where P_T = the signal power
 θ = the phase modulation sensitivity
 $m(t)$ = the modulating function.

The modulating function $m(t)$ is usually a modulated sinusoidal subcarrier. For the sake of keeping the ensuing development as simple as possible, and without loss of the general concept, it will be assumed that $m(t)$ is a unit amplitude "square" type function (for example, a digital data

Table 1. A List of Sampled Data Measurements

Payload Simulator Subsystem	Type of Measurement	Display/Units
Transponder Receiver	Noise Figure	dB
	Carrier Suppression	dB, or deviation angle
	Carrier to Noise Spectral Density Ratio	dB
	Phase Detector Noise Biasing	millivolts
	Ranging SNR*	dB
	AGC Level	volts, or millivolts
	Optimum Phase Detector Reference Phasing*	dB, or volts
Transponder Transmitter	Carrier Suppression*	dB
	Phase Noise*	RMS degrees or radians
Telemetry Modulator	FM Deviation*	Hz, or kHz
Command Detector Unit	NASA Bit SNR	dB
	NASA Bit Error Probability	Number
	SGLS Symbol SNR	dB
All Subsystems	Filter Response	Hz, or kHz
	Filter Noise Bandwidth	Hz, or kHz

* Requires additional capability in the Payload Simulator subsystems beyond that described in Sections 4.1 and 4.3 (see text for explanations).

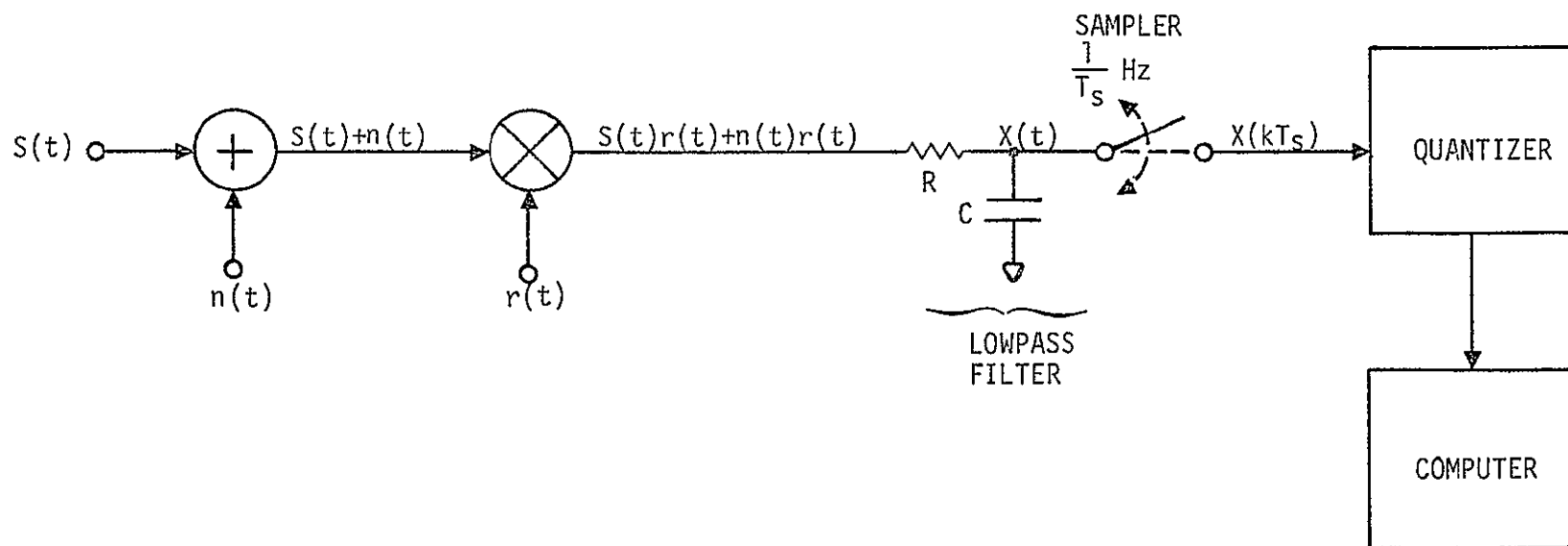


Figure 1. Sampled Data Measurement Model

stream) Thus, (1) may be further developed as

$$\begin{aligned} S(t) &= \sqrt{2P_T} \cos(\theta) \cos(\omega_0 t) - \sqrt{2P_T} \sin(\theta) m(t) \sin(\omega_0 t) \\ &= \sqrt{2P_C} \cos(\omega_0 t) - \sqrt{2P_m} m(t) \sin(\omega_0 t), \end{aligned} \quad (2)$$

where P_C = residual carrier power = $P_T \cos^2(\theta)$
 P_m = modulation sideband power = $P_T \sin^2(\theta)$.

The additive noise will be represented by the usual wideband bandpass model, viz.,

$$n(t) = n_c(t) \cos(\omega_0 t) - n_s(t) \sin(\omega_0 t), \quad (3)$$

where $n(t)$ has a two-sided noise spectral density of $N_0/2$ watts/Hz in the general vicinity of ω_0 , and $n_c(t)$ and $n_s(t)$ are independent lowpass noise components, each with two-sided noise spectral density of N_0 watts/Hz.

Reference signal to the phase detector or multiplier will be defined as

$$r(t) = \sqrt{2} \cos[\omega_0 t + \varphi], \quad (4)$$

where φ is an arbitrary phase angle.

The resulting phase detector output, neglecting the $2\omega_0$ terms, is

$$\begin{aligned} S(t)r(t) + n(t)r(t) &= \sqrt{P_C} \cos(\varphi) - \sqrt{P_m} \sin(\varphi) m(t) \\ &\quad + \frac{\sqrt{2}}{2} \cos(\varphi) n_c(t) - \frac{\sqrt{2}}{2} \sin(\varphi) n_s(t). \end{aligned} \quad (5)$$

When $\varphi = 0$, the AGC detector of Section 4.1.3.5 is realized, and when $\varphi = \pi/2$, the command demodulator (4.1.3.4) or ranging demodulator (4.1.3.7) is obtained.

A single section RC lowpass filter (LPF) is employed to smooth the phase detector output. Most importantly, this filter establishes the noise power of the subsequent sample values. The exact form of this filter is not important; what matters is that its noise bandwidth be accurately known and that its 3 dB frequency be selected to best serve the sampled data measurement being conducted. The two-sided noise bandwidth of an ideal RC LPF is

$$2B_n = \pi f_{3\text{ dB}} = \frac{1}{2RC} . \quad (6)$$

Output from the LPF is sampled at a rate of $1/T_s$ Hz where, in order to guarantee virtual independence of samples, T_s is determined according to the relationship

$$T_s \cong 4RC . \quad (7)$$

An exact equality between $4RC$ and T_s is not required, only the order of magnitude indicated by (7).

If the output of the LPF is represented by the function $X(t)$, the sample values may be designated $X(nT_s)$, $n=1,2,3,\dots$

In an actual sampled data system mechanization, the samples are quantized over a selected range of discrete values, each sample thus being represented as a K-bit binary number. An analog-to-digital converter (ADC) performs this function and, for measurements of the type indicated in Table 1, $K=8$ (seven magnitude bits plus a sign bit) is sufficient.

The computer (whether it be a microprocessor or other type of machine) operates on the quantized $X(nT_s)$ values to compute the desired quantity. In some cases, as will be explained below, additional computer input is required in order to conduct the particular measurement. The subsequent sections of this appendix will deal with the nature of the various measurement algorithms.

3.0 CARRIER AGC LEVEL, SUPPRESSION, AND SNR MEASUREMENT

With $\varphi = 0$, the output of the LPF may be expressed as

$$X(t) = \sqrt{P_c} + \frac{\sqrt{2}}{2} n_{cf}(t) , \quad (8)$$

where the symbol $n_{cf}(t)$ indicates the lowpass filtered version of $n_c(t)$.

Because $n_{cf}(t)$ is a random noise voltage, the statistical expected value of $X(t)$ is

$$\overline{X(t)} = \sqrt{P_c} . \quad (9)$$

Now, since the entire process will be assumed as stationary (for the types of measurements to be made in regard to the Payload Simulator, this is a reasonable assumption), the time average, in the limit, gives

the same result, viz.,

$$\lim_{T \rightarrow \infty} \langle X(t) \rangle_T = \sqrt{P_C} . \quad (10)$$

Here, the triangular brackets $\langle \rangle$ indicate the time average and T is the finite time period over which the average is made.

For the finite time average, results exactly equal to the expected or limiting time average will not be obtained, thus the expression

$$\langle X(t) \rangle_T \rightarrow \sqrt{P_C} \quad (11)$$

will be written with the understanding that, as $T \rightarrow \infty$, the symbol \rightarrow may be replaced by the symbol $=$.

In terms of equalities,

$$\langle X(t) \rangle_T = \sqrt{P_C} + \frac{\sqrt{2}}{2} \langle n_{cf}(t) \rangle_T ; \quad (12)$$

therefore $\langle X(t) \rangle_T$ is a random variable whose variance arises from $\langle n_{cf}(t) \rangle_T$. The accuracy with which $\langle X(t) \rangle_T$ gives a measure of $\sqrt{P_C}$ thus depends on the relative strength of the noise term and on how long it is averaged. Such accuracy is often expressed in terms of confidence intervals, which in turn are related to the relative strength and averaging time. Confidence interval curves have been generated for many types of statistical measurement techniques.

The sampled data time average may be written as

$$\langle X(nT_S) \rangle_N \triangleq \mu_N = \frac{1}{N} \sum_{n=1}^N X(nT_S) \rightarrow \sqrt{P_C} . \quad (13)$$

N samples are averaged by the computer via the indicated operation, yielding the measure of the RMS carrier voltage, represented by the new symbol, μ_N .

Since $\mu_N \rightarrow \sqrt{P_C}$, this sampled data measurement gives an indication of the receiver open AGC loop (i.e., fixed gain receiver) residual carrier level. Obviously, in a real receiver, $\mu_N \rightarrow G_R \sqrt{P_C}$, where G_R is the receiver gain from the point of signal input to the sampled data LPF output. Referring to Figure 4-3 in the main body of this report, the samples may be taken at the output of the AGC LPF

($RC = 0.005$ sec), with the AGC loop in the "manual gain" position. Setting the manual gain control at a known position so that G_R is established, the values of G_R and the AGC "bias" term may be input to the computer, and the computational algorithm will proceed to generate the desired result. The computer can display the result in millivolts, milliwatts, or dBm, as desired.

Much of the time, the AGC is measured closed-loop. Under this condition, the AGC voltage is no longer directly proportional to the carrier level. The closed-loop AGC characteristic may, however, be measured, quantized and stored in the computer memory (ROM, if a microprocessor is used). The sampled data algorithm is then structured to compare the averaged samples with the stored characteristic, make necessary conversions and computations, and display the result. This, of course, may be done continuously while the receiver is tracking and otherwise being used in an operational manner. Thus, routine carrier signal level monitoring in absolute units is possible.

Carrier suppression may be easily established using the AGC samples. Although the measurement may be made open-loop or closed-loop, better accuracy is obtained open-loop. The receiver signal level is set to be "strong," and the receiver gain is adjusted to give linear operation with the no-modulation AGC voltage near the maximum of the ADC quantizer range. (Note that the computer algorithm may also be structured to indicate maximum or overload conditions.) Modulation is removed from the carrier, and the computer is instructed that the no-modulation level is to be measured and retained. The computer is then placed in the "display carrier suppression" mode, where the ratio between the averaged AGC samples and the no-modulation level is calculated and displayed (usually in dB) in a periodic manner (updated, say, every 0.5 sec). The modulation may be applied to the carrier and adjusted, and the resulting carrier suppression directly read. If the modulating signal is "square" in nature, the computer algorithm is determining $\cos(\theta)$ [see (2)], from which θ may be calculated and displayed. When the modulating signal is sinusoidal, $J_0(\theta_{\text{peak}})$ is being measured, etc.

Finally, the carrier signal-to-noise spectral density ratio may be determined from the AGC samples. Again, this may be accomplished open- or closed-loop. If the average of the square of the samples is

calculated, the following result is obtained.

$$\langle X^2(nT_s) \rangle \triangleq \eta_N^2 = \frac{1}{N} \sum_{n=1}^N X^2(nT_s) \rightarrow P_c + \frac{1}{2} \sigma_{n_{cf}}^2, \quad (14)$$

where $\sigma_{n_{cf}}^2$ = variance of the filtered noise term = $N_0/2RC$. The computer then calculates the following expression:

$$\frac{1}{2RC} \left[\frac{\mu_N^2}{\eta_N^2 - \mu_N^2} \right] \rightarrow \frac{P_c}{N_0}. \quad (15)$$

The accuracy is proportional to the averaging time, or the index N. Display may be in dB, and the ratio can also be converted into any other useful form, such as signal-to-noise ratio in the phase-locked loop tracking bandwidth.

4.0 NOISE FIGURE MEASUREMENT

Receiver noise figure is usually measured using a calibrated noise source attached to the receiver input terminals and a noise figure meter which very accurately measures the receiver noise power at an IF level. To obtain the requisite accuracy, the noise power detector is a bolometer or other calorimetric type device, requiring that the IF be 50 MHz or higher for good results. Generally, noise figure meters are expensive and have no use beyond their intended function.

A sampled data algorithm may be used to determine noise figure. Let the receiver AGC detector be the device from which the samples are taken. All signals are removed from the receiver input and the input port is terminated in its characteristic impedance. The receiver is tuned to the desired receive frequency, but since no tracking is possible, φ in (4) is a random variable uniformly distributed on $(0, 2\pi)$. Under these conditions, $X(t)$ is

$$X(t) = \frac{\sqrt{2}}{2} [\cos(\varphi) n_{cf}(t) - \sin(\varphi) n_{sf}(t)]. \quad (16)$$

The expected value of $X^2(t)$ may be straightforwardly shown to be

$$\begin{aligned}\overline{X^2(t)} &= \frac{1}{2} [\overline{\cos^2 \varphi} \overline{n_{cf}^2(t)} + \overline{\sin^2 \varphi} \overline{n_{sf}^2(t)}] \\ &= \frac{N_0}{2RC} \triangleq P_1.\end{aligned}\quad (17)$$

Note that the result is independent of φ .

Now assume that a noise generator with a known noise spectral density of $N_c/2$ watts/Hz is connected to the receiver input terminals. Since the noise produced by this generator and the receiver internal noise are independent, the expected value of $X^2(t)$ now becomes

$$\overline{X^2(t)} = \frac{1}{2RC} (N_0 + N_c) \triangleq P_2. \quad (18)$$

The receiver noise figure is then calculated from the relationship:

$$NF = \left(\frac{2P_1}{P_2} \right) \left(\frac{N_c}{kT_0} \right) = \left(\frac{2P_1}{P_2} \right) NF_c, \quad (19)$$

where $(kT_0) = 4 \times 10^{-18}$ mw/Hz ($= -174$ dBm/Hz), and NF_c is the noise figure of the calibrated noise generator.

Since the computer algorithm will calculate the exact square of the samples and compute the appropriate expression in (19), very accurate noise figure determination is obtained via the sampled data approach. Note that, aside from a different stored program within the computer, no sampled data capability beyond that required to perform operations discussed in Section 3.0 is required.

5.0 PHASE DETECTOR NOISE BIAS MEASUREMENTS

Phase detectors often exhibit direct voltage outputs when large noise voltages are applied to their inputs. A sampled data algorithm may be used to check for this condition. With no signal input to the receiver and with the receiver gain set to a value which produces maximum noise drive to the phase detector (short of producing overt compression), a very long term average is made of the samples.* Also, the RMS value of the samples is calculated. The average to RMS value is computed

*The samples must be taken directly from the phase detector with no intervening dc amplifier.

and expressed in dB. If the result is larger than -50 dB, a possible phase detector noise bias problem exists.

6.0 RANGING SNR MEASUREMENTS

Since the ranging signal at the output of the ranging phase detector consists of a periodic sinusoid or square-wave, the most expedient means for measuring ranging SNR is to sample the signal component only at its positive maximum value. Thus, the signal peak value is obtained which, in turn, may be related to the signal power via the computational algorithm. The SNR is determined as in Section 3.0.

In order to perform a measurement of this type, it is necessary to provide the ADC with a timing signal that has the proper ranging signal phase relationship.

7.0 TRANSMITTER CARRIER SUPPRESSION MEASUREMENT

The Payload Simulator transmitter carrier suppression may be measured with the same type of procedure outlined in Section 3.0.

What is required for this measurement is a coherent phase detector capable of demodulating the output of the X8 multiplier in the transmitter chain of Figure 4-3. Figure 2 shows the circuits that would have to be added to the transmitter architecture of Section 4.1 in the main report. In Figure 2, the solid boxes are taken from Figure 4-3, and the broken-line boxes are the necessary additions. The adjustable phase-shifter is needed to place the phase detector reference in-phase with the phase modulator residual carrier component.

8.0 NASA CDU BIT SNR MEASUREMENT

In the digital mechanization of the CDU discussed in Section 4.2.4 of the main report, the bit detector matched filter value at the end of the bit integration period is already a digital number. The magnitude or absolute value of this number, taken over a sufficient number of bits, supplies a measure of the command detector figure-of-merit, E_b/N_0 .

Designating the matched filter numbers as X_m , the following variables are calculated:

$$\hat{\mu} = \frac{1}{M} \sum_{m=1}^M X_m \quad (20)$$

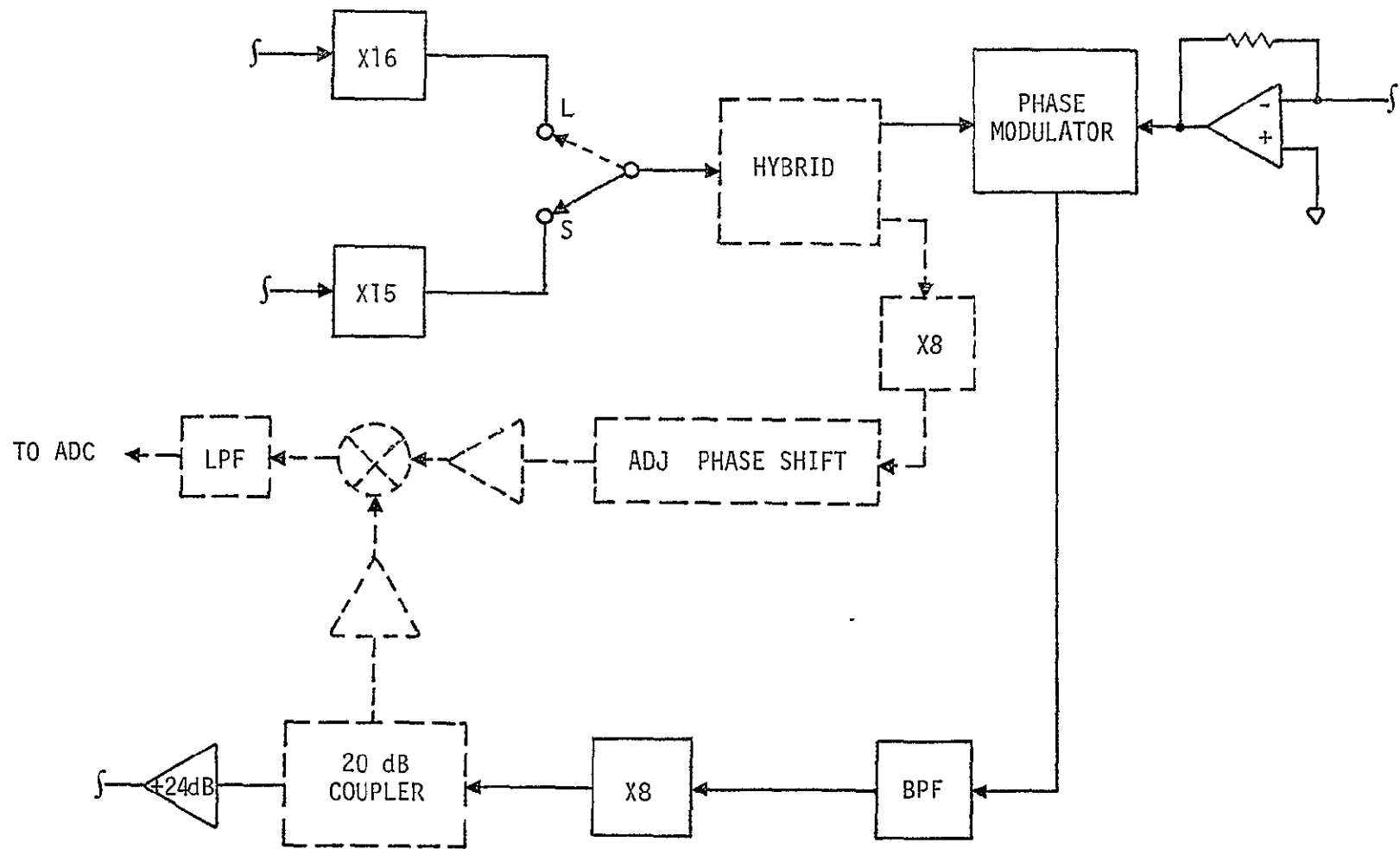


Figure 2. Transmitter Additions for Carrier Suppression Measurement

$$\text{and} \quad \hat{\sigma}^2 = \frac{1}{M-1} \sum_{m=1}^M (X_m - \hat{\mu})^2. \quad (21)$$

The matched filter SNR estimate is then defined by the relationship:

$$2 \widehat{E_b/N_0} \triangleq \hat{\mu}^2 / \hat{\sigma}^2. \quad (22)$$

This measure of matched filter SNR is quite accurate for values greater than 4 dB. For smaller values, a correction factor may be applied by the computer.

If it is assumed that the matched filter noise is Gaussian (which it should be for all practical situations of interest), the expected bit error probability may be calculated in the computer from the equation.

$$\widehat{p_e^b} = \frac{1}{2} \operatorname{erfc} \left[\sqrt{\widehat{E_b/N_0}} \right]. \quad (23)$$

APPENDIX D
SGLS COMMAND WAVEFORM

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SGLS COMMAND WAVEFORM

This appendix describes the structure of the SGLS command waveform and shows functionally how it may be generated.

SGLS commands are transmitted using one of three discrete tone frequencies, each T_s sec long. The command symbol and frequency relationships are:

<u>Symbol</u>	<u>Tone Frequency</u>
"1"	$f_A = 95 \text{ kHz}$
"0"	$f_B = 76 \text{ kHz}$
"S"	$f_C = 65 \text{ kHz}$

Symbol rates are 1000 and 2000 symbols per second (sps), corresponding to $T_s = 1 \text{ ms}$ and 0.5 ms , respectively.

Figure 1 shows the command waveform. The composite symbol tone signal is amplitude modulated by a rate waveform whose fundamental frequency is one-half the symbol rate. At 1000 sps, the rate waveform is triangular and, at 2000 sps, it is sinusoidal.

The modulation factor is given in terms of E_{\max} , E_{\min} and E_0 as

$$\frac{E_{\max} - E_{\min}}{E_0} = 0.5.$$

The phase of the modulating rate waveform is given by T_D relative to the start of the symbol period and the midpoint or zero crossing of the rate waveform as

$$T_D = 0.6 T_s.$$

Expressed as an equation at the 2000 sps rate, the command waveform is

$$\sqrt{2P_s} \{1 + \sqrt{0.0625} \sin [2\pi \times 1000 t - 0.6 \pi]\} \sin [2\pi f_1(t) t],$$

where P_s = tone power

f_1 = instantaneous tone frequency.

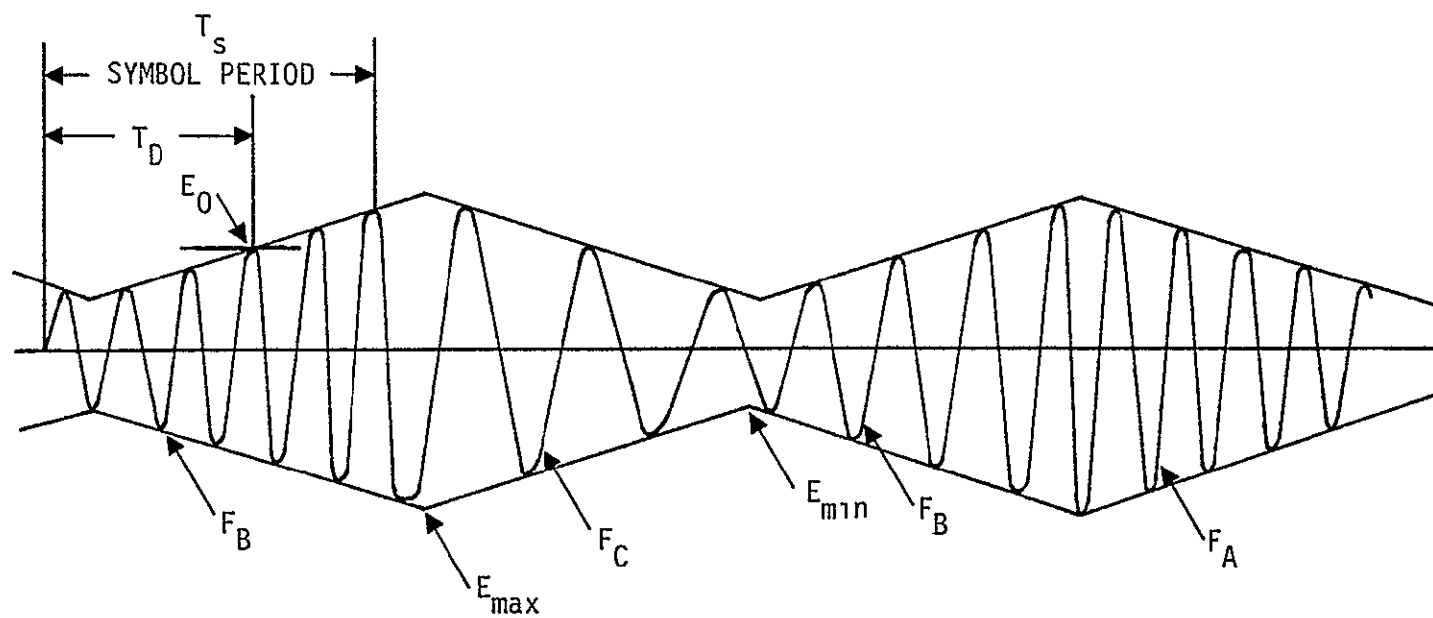


Figure 1. SGLS Command Waveform

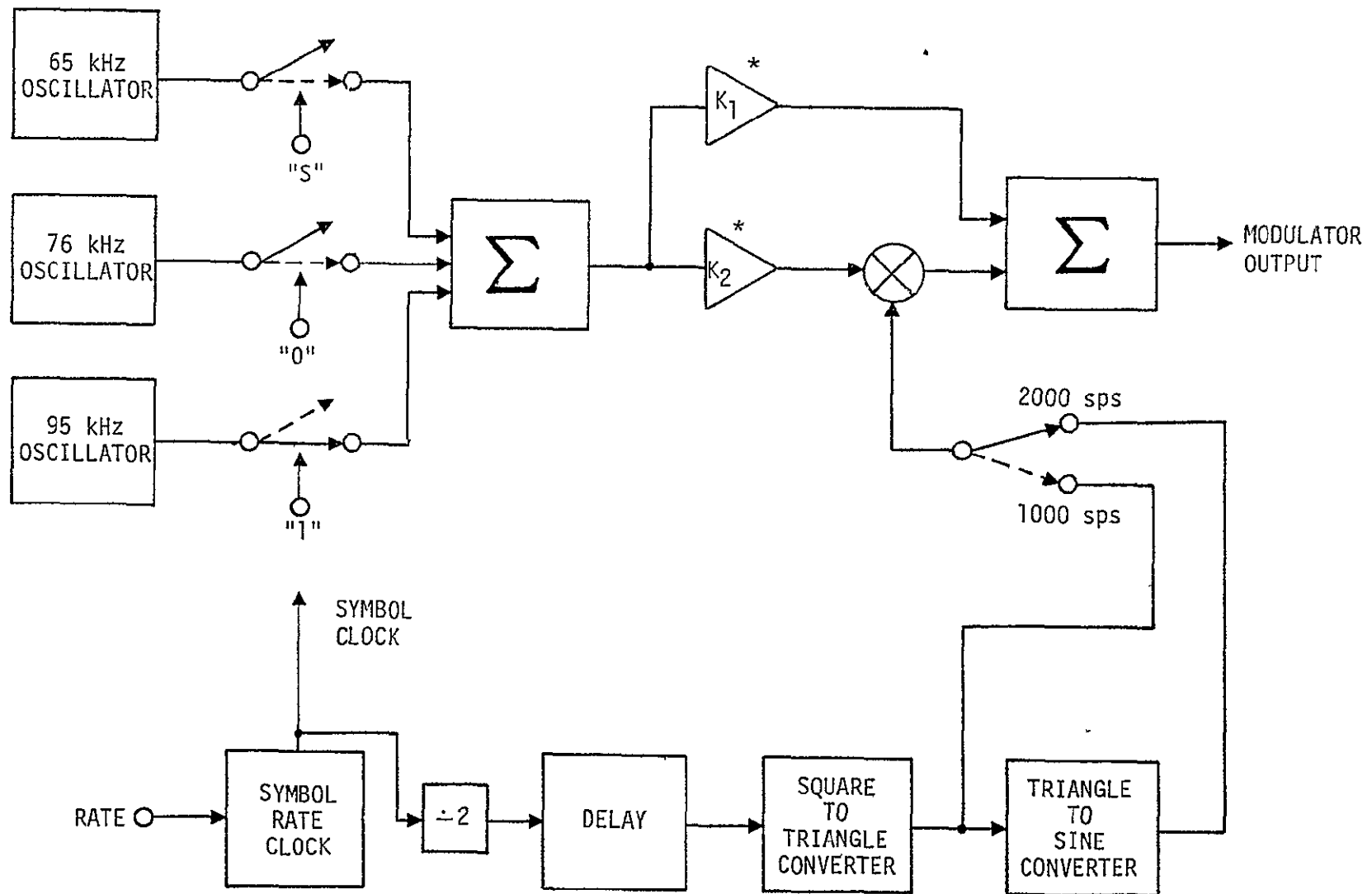
At the 1000 sps rate, the equation is similar, but the modulating waveform at a fundamental frequency of 500 Hz is triangular (and mathematically expressible as a Fourier series).

Table 1 gives the tone and rate waveform power components relative to the total SGLS command power.

Table 1. Relative Component Powers

Symbol Rate	Tone to Total Power	Rate Waveform to Total Power
1000	-0.09 dB	-16.9 dB
2000	-0.13 dB	-15.2 dB

Figure 2 shows a functional block diagram of how the SGLS command modulator may be realized.



* K_1 and K_2 are selected to give the proper tone and rate waveform powers

Figure 2 Functional SGLS Command Modulator